Nanoscale III-V Electronics: from Quantum-Well Planar MOSFETs to Vertical Nanowire MOSFETs

J. A. del Alamo

Microsystems Technology Laboratories, MIT

Purdue University,

West Lafayette, IN; September 29, 2015

Acknowledgements:

- D. Antoniadis, J. Lin, W. Lu, A. Vardi, X. Zhao
- Sponsors: DTRA, Lam Research, Northrop Grumman, NSF, Samsung
- Labs at MIT: MTL, EBL

Contents

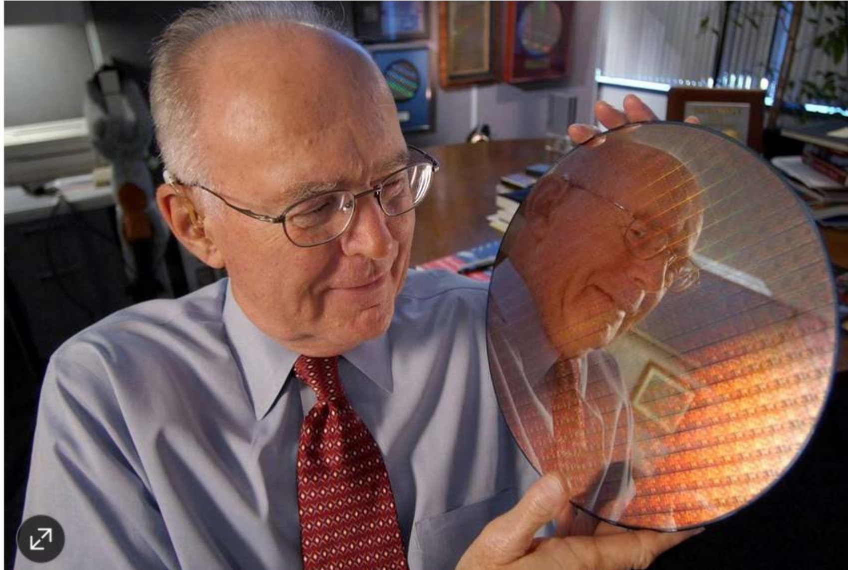
1. Motivation: Moore's Law and MOSFET scaling
2. Planar InGaAs MOSFETs
3. InGaAs FinFETs
4. Vertical nanowire InGaAs MOSFETs
5. Conclusions

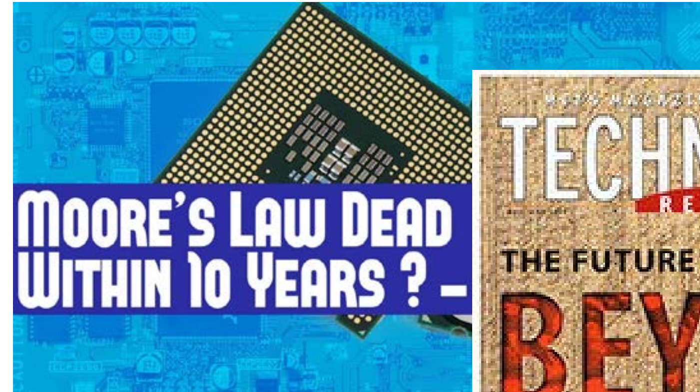
1. Moore's Law at 50: the end in sight?

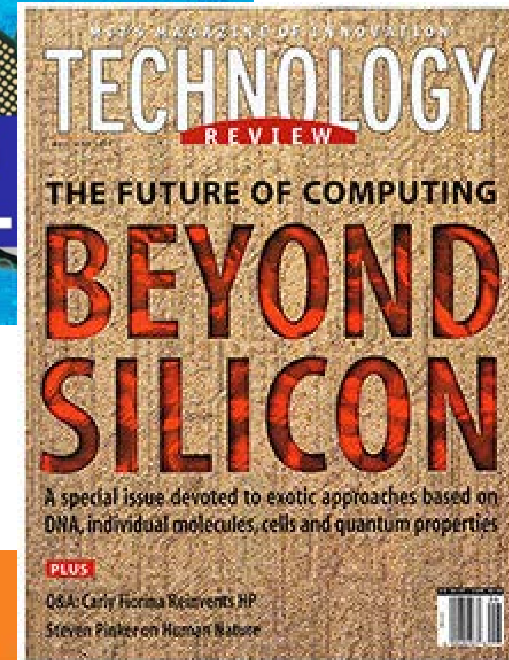
THE WALL STREET JOURNAL.

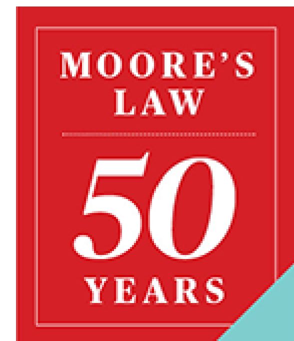
Moore's Law Is Showing Its Age

The prediction about squeezing transistors onto silicon has been revised again.



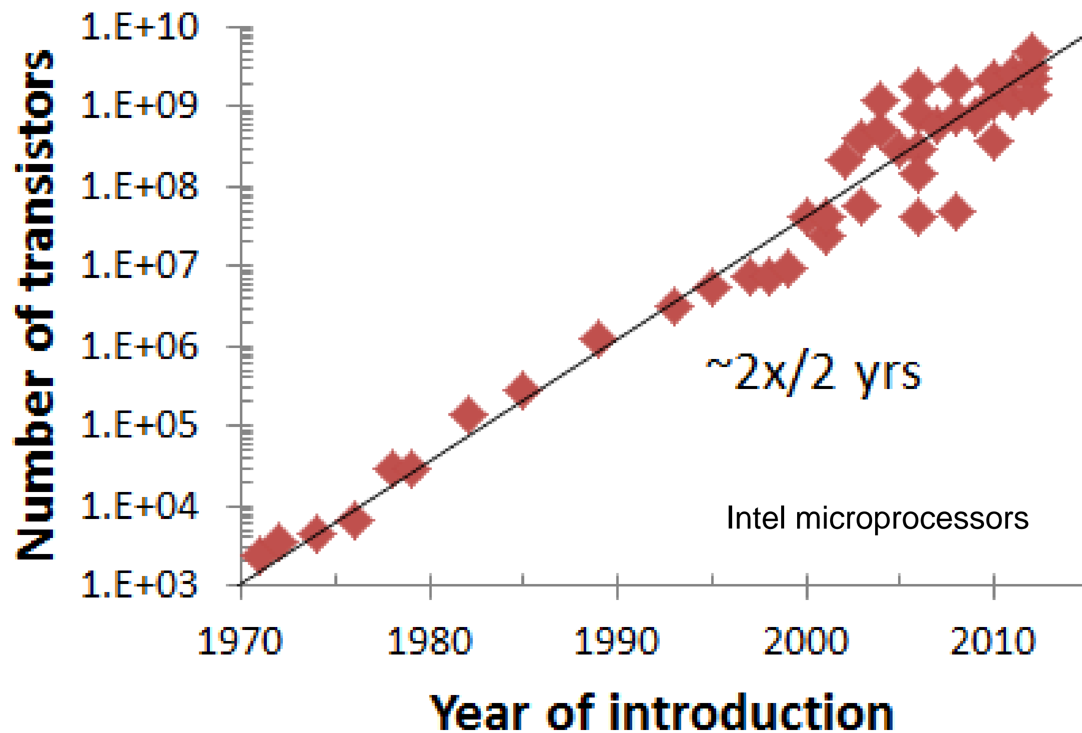


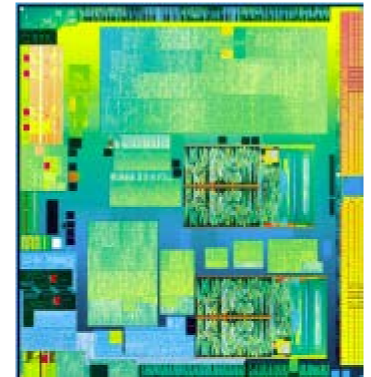




Moore's Law

Moore's Law = exponential increase in transistor density

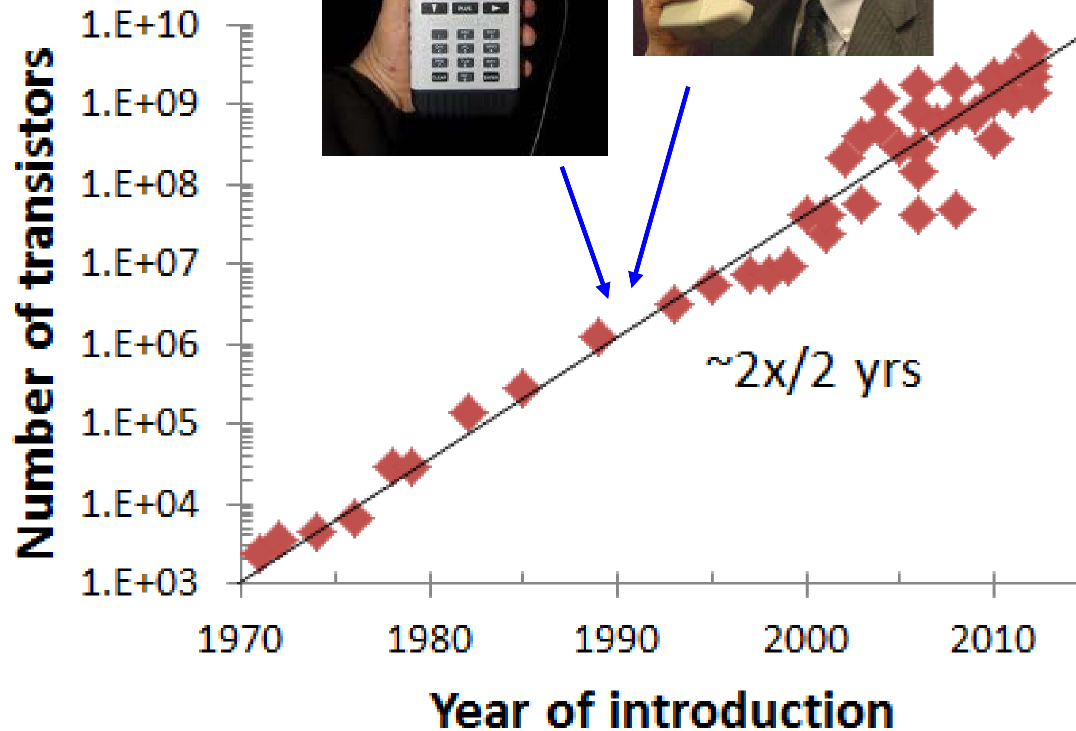




What if Moore's Law had stopped in 1990?

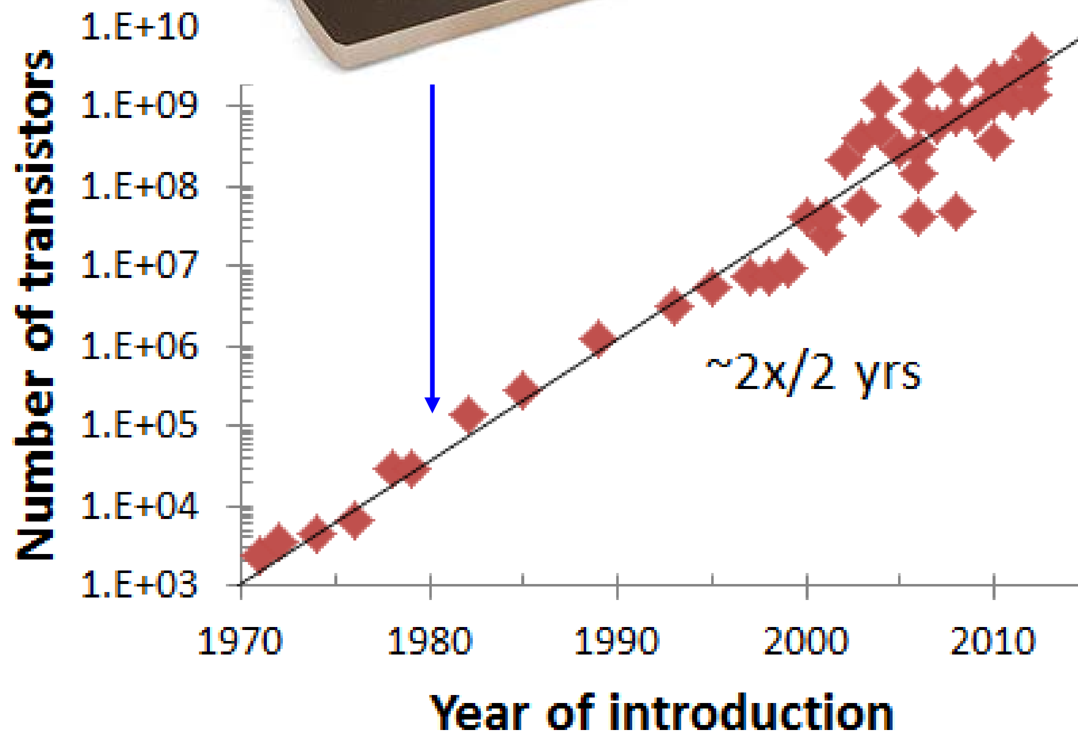
GPS handheld device circa 1990

Cell phone circa 1990

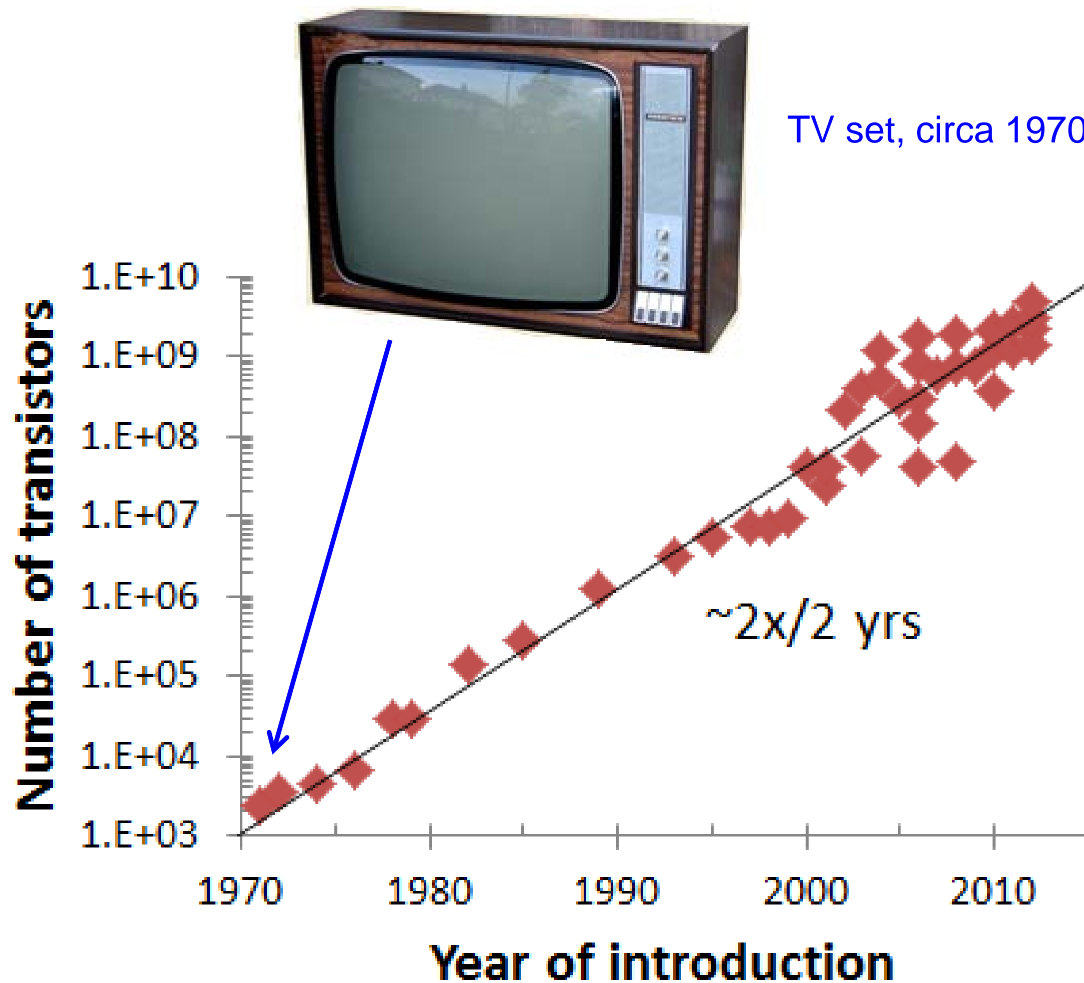


What if Moore's Law had stopped in 1980?

Laptop computer circa 1981



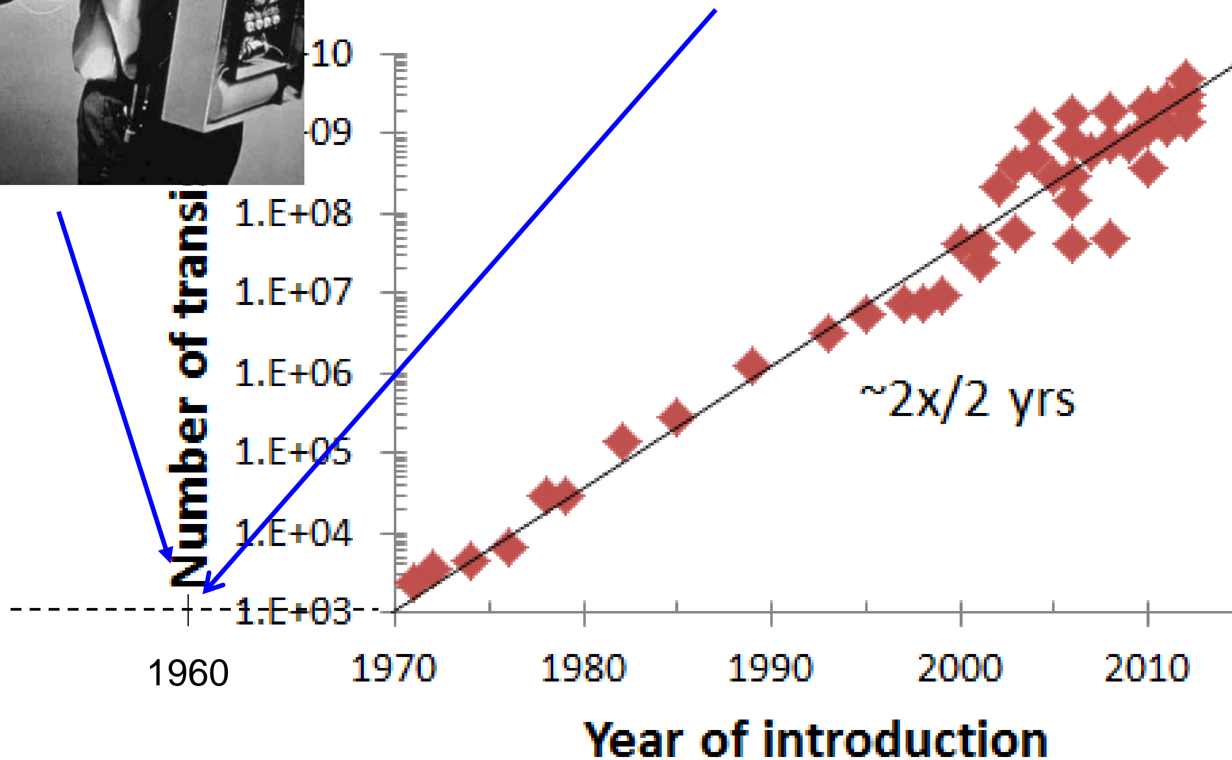
What if Moore's Law had stopped in 1970?



What if Moore's Law had never happened?

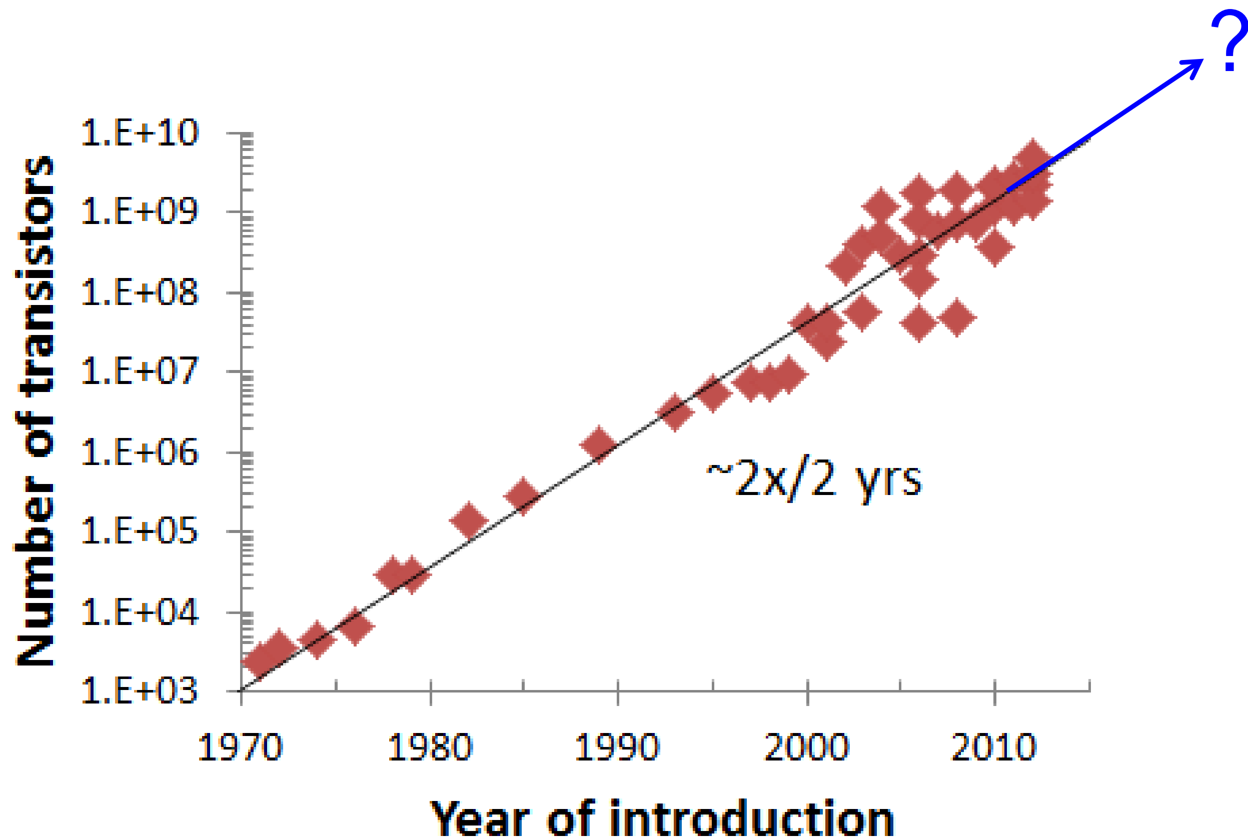
Insulin pump circa 1960

"Personal calculator" circa 1960



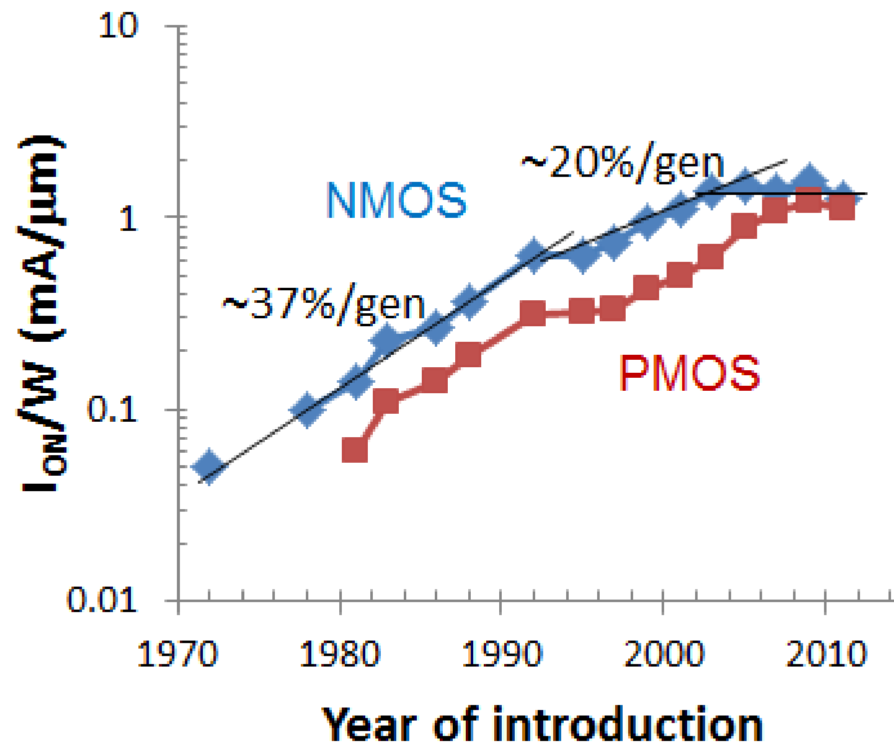
Moore's Law

How far can Si support Moore's Law?



Transistor scaling → Voltage scaling → Performance suffers

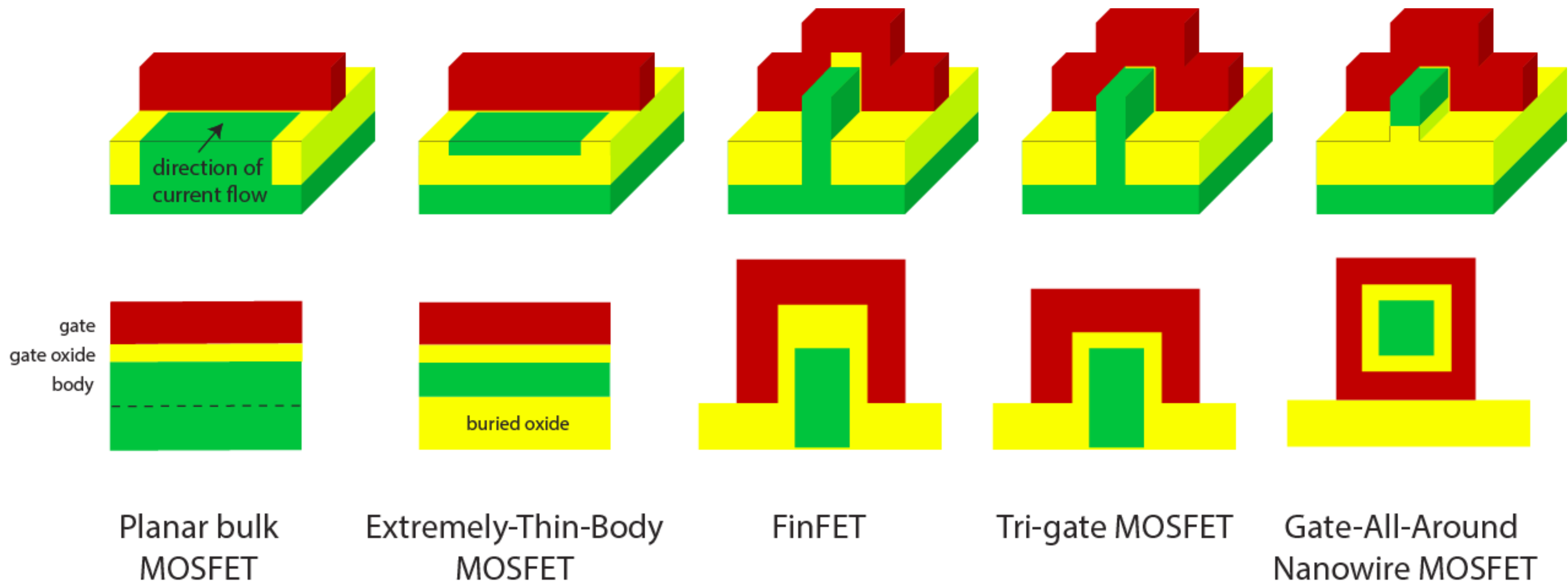
Transistor current density (planar MOSFETs):



Transistor performance saturated in recent years

Moore's Law: it's all about MOSFET scaling

1. New device structures:



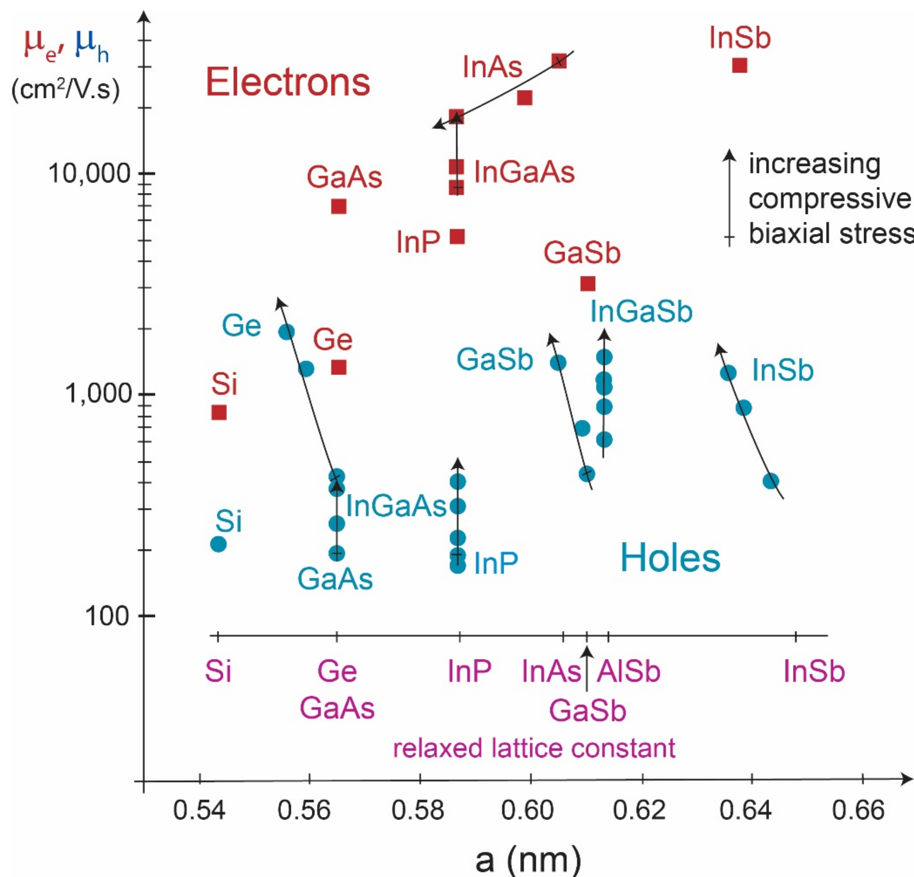
Enhanced gate control → improved scalability

Moore's Law: it's all about MOSFET scaling

2. New materials:

Si → Strained Si → SiGe → InGaAs

Si → Strained Si → SiGe → Ge → InGaSb

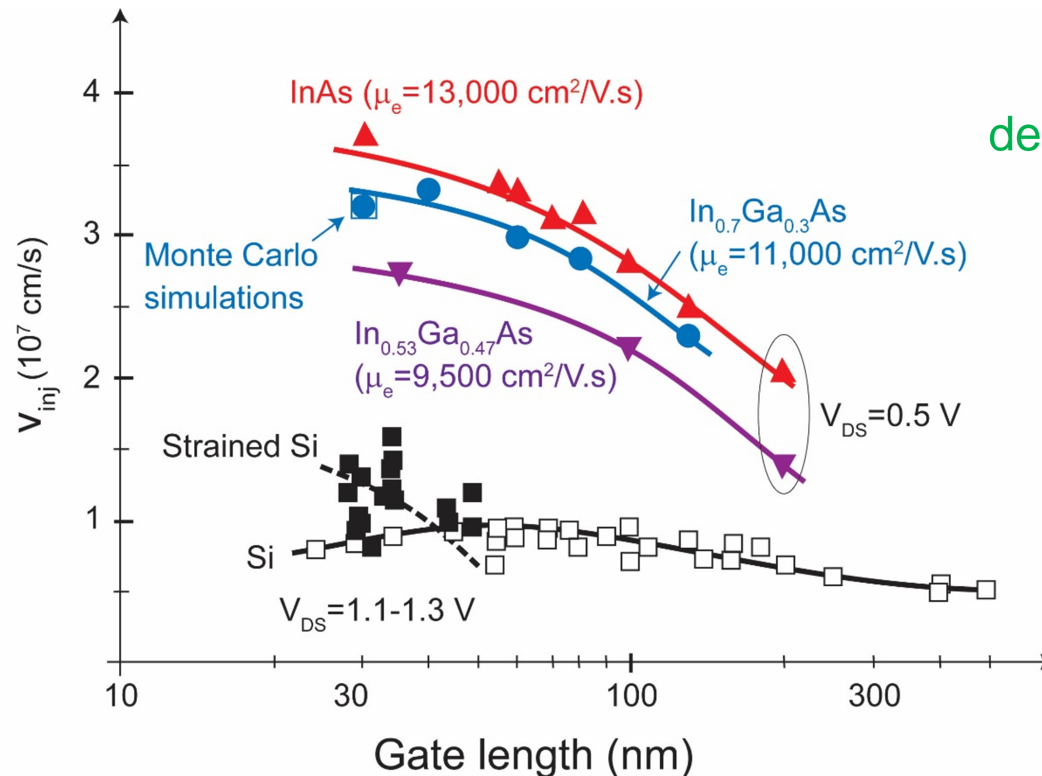


Future CMOS might involve two different channel materials with <u>two different relaxed lattice constants</u>!

del Alamo, Nature 2011 (updated)

Electron velocity: InGaAs vs. Si

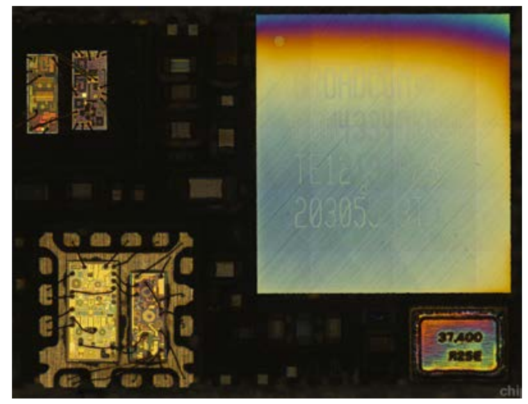
Measurements of electron injection velocity in HEMTs:

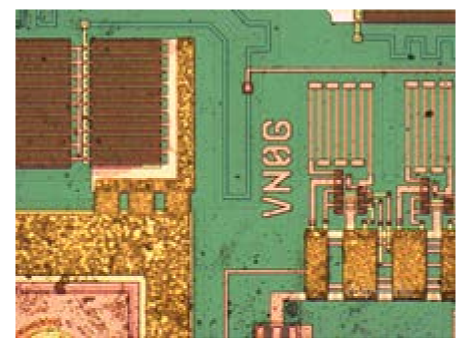


del Alamo, Nature 2011

- v_{inj}(InGaAs) increases with InAs fraction in channel
- v_{inj}(InGaAs) > $2v_{inj}$(Si) at less than half V_{DD}
- ~100% ballistic transport at L_g~30 nm

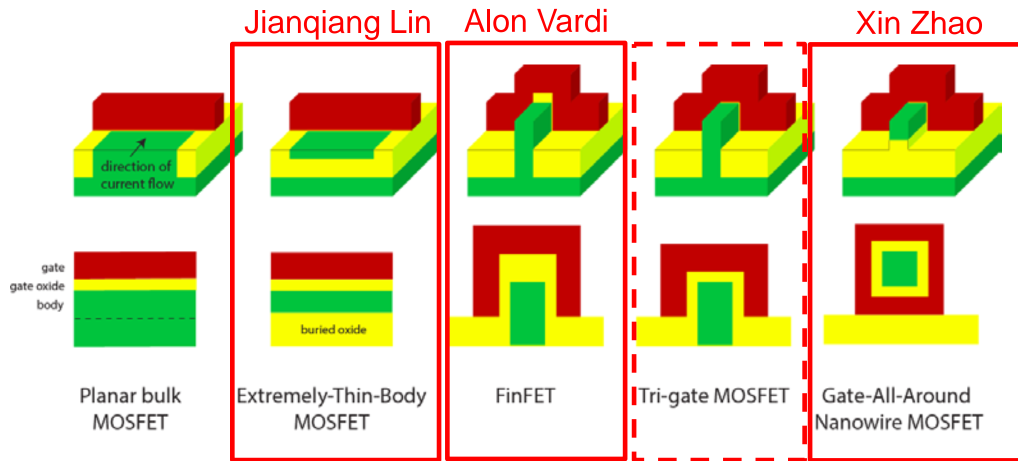
III-V electronics in your pocket!





del Alamo's group at MIT: Current and future activities

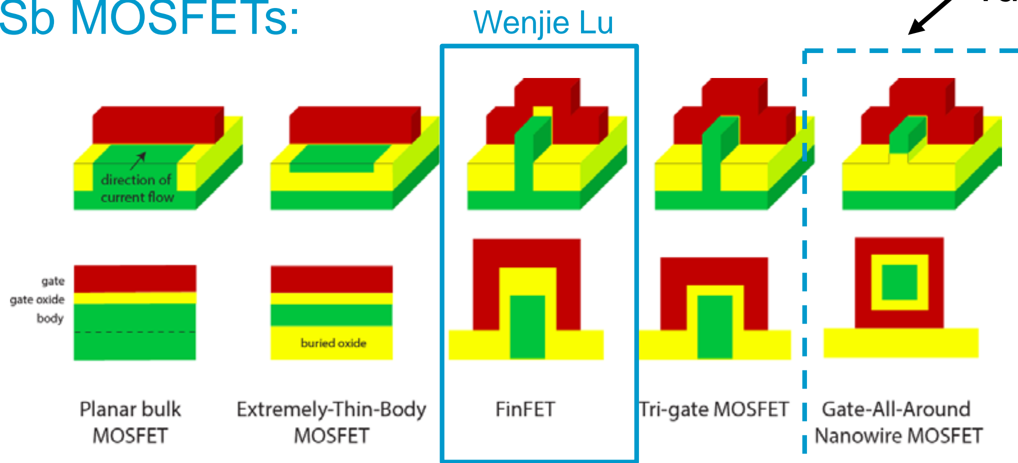
N-type InGaAs MOSFETs:



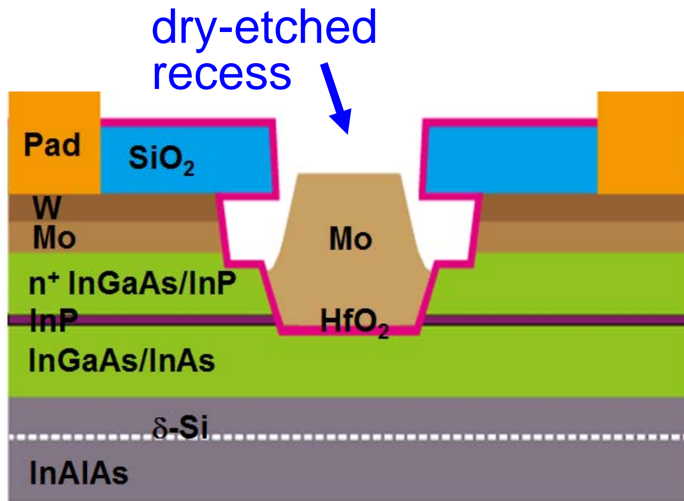
New students:
Xiaowei Cai
Dongsung Choi

future

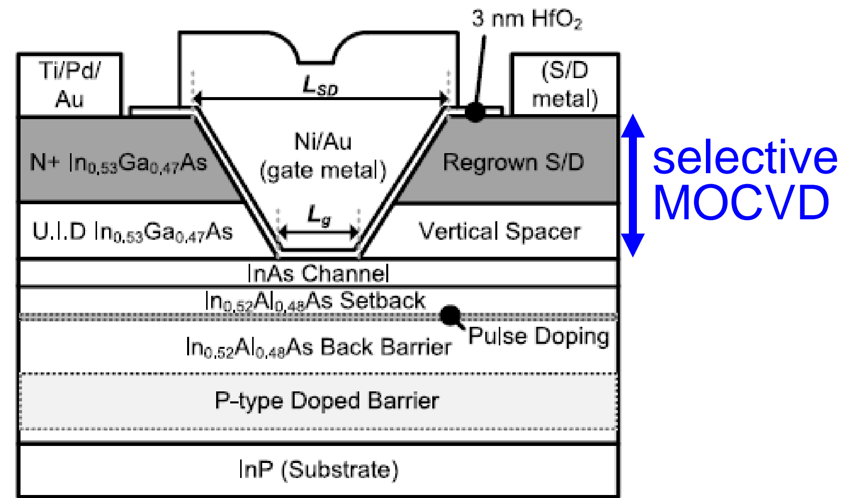
P-type InGaSb MOSFETs:



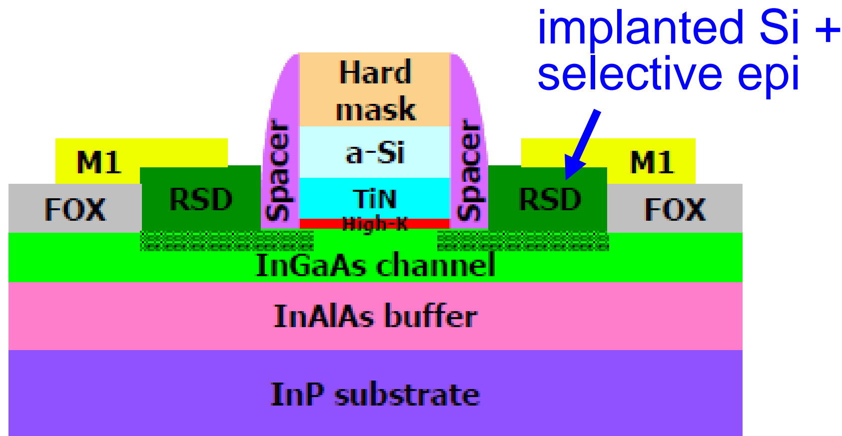
2. Self-aligned Planar InGaAs MOSFETs



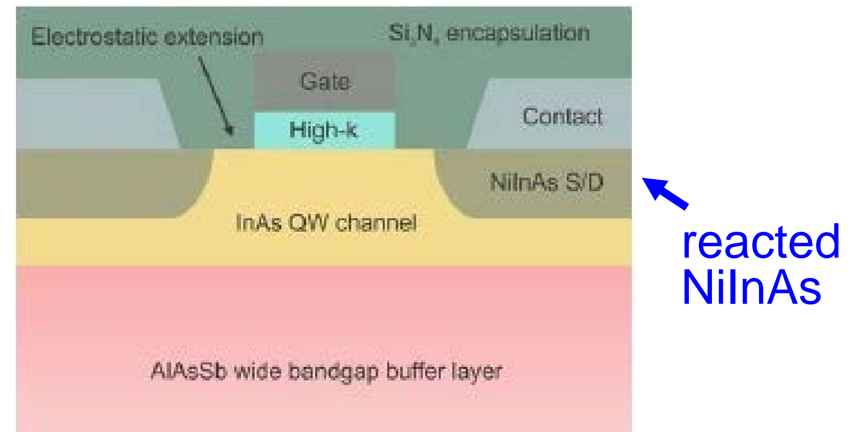
Lin, IEDM 2012, 2013, 2014



Lee, EDL 2014; Huang, IEDM 2014

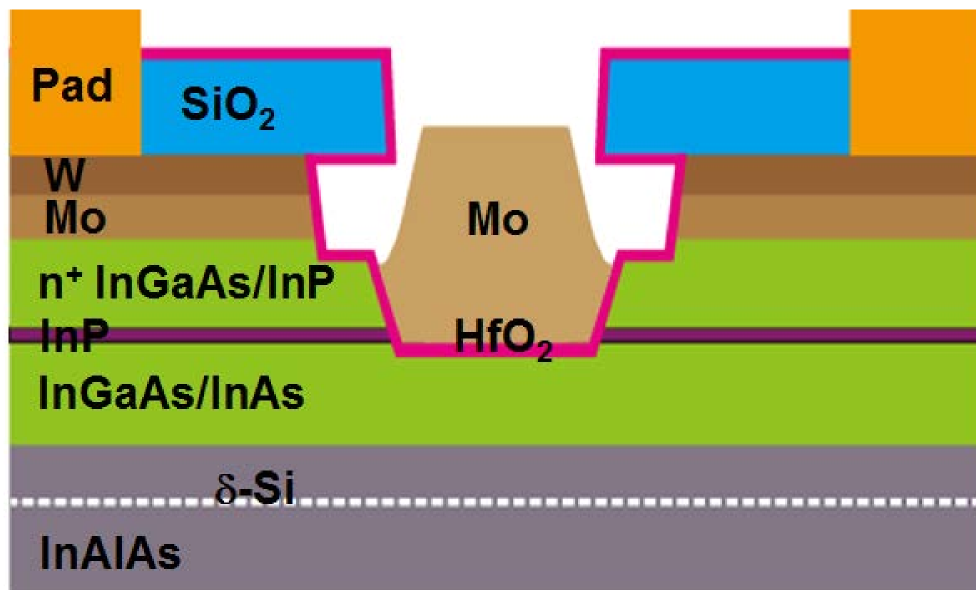


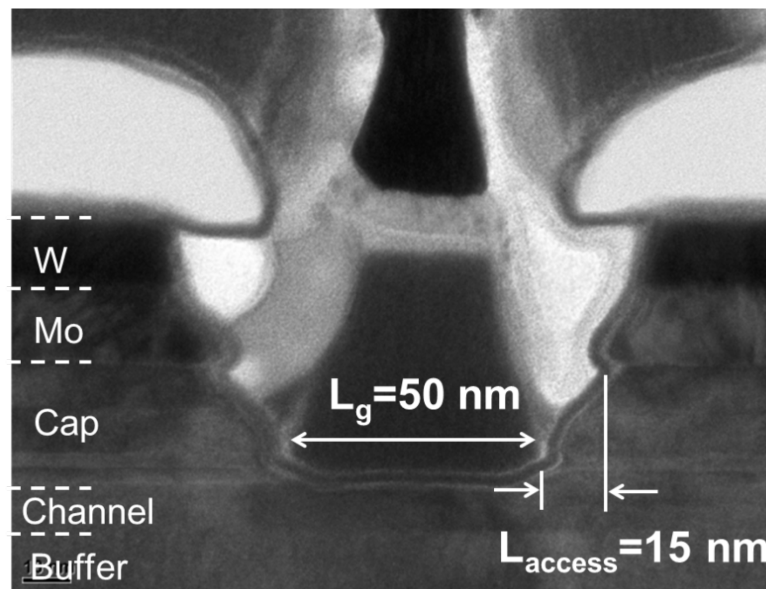
Sun, IEDM 2013, 2014



Chang, IEDM 2013

Self-aligned Planar InGaAs MOSFETs @ MIT





Lin, IEDM 2012, 2013, 2014

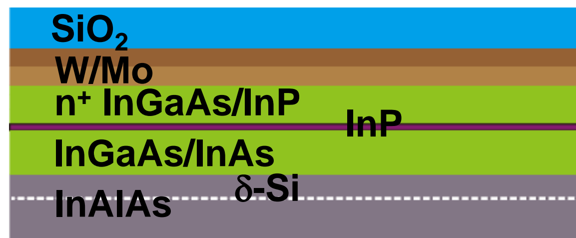
Jerome Lin

Recess-gate process:

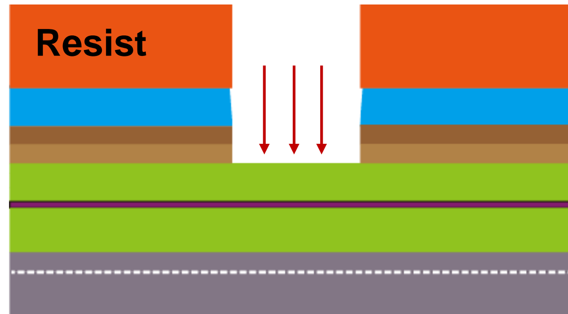
- CMOS-compatible
- Refractory ohmic contacts (W/Mo)
- Extensive use of RIE

Fabrication process

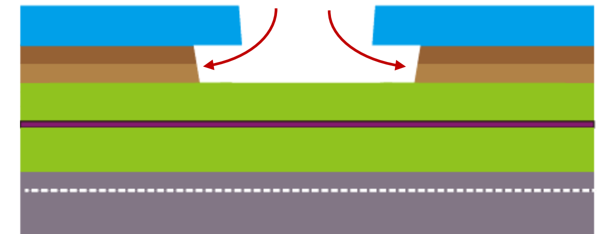
Mo/W ohmic contact
+ SiO_2 hardmask



SF_6, CF_4 anisotropic RIE

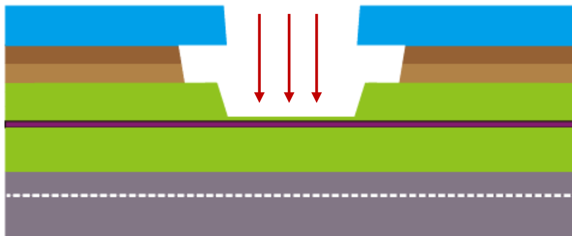


CF_4:O_2 isotropic RIE

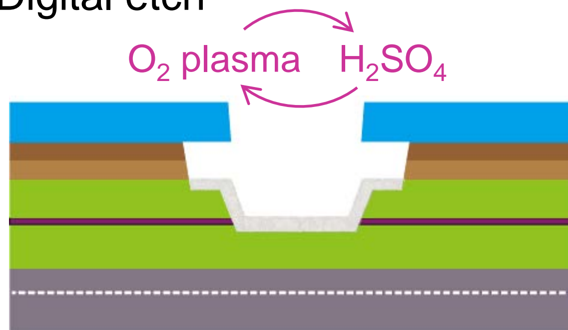


Waldron, IEDM 2007

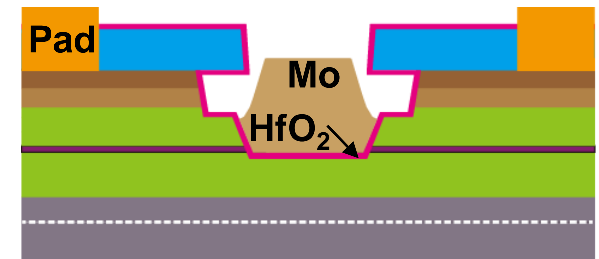
Cl_2:N_2 anisotropic RIE



Digital etch



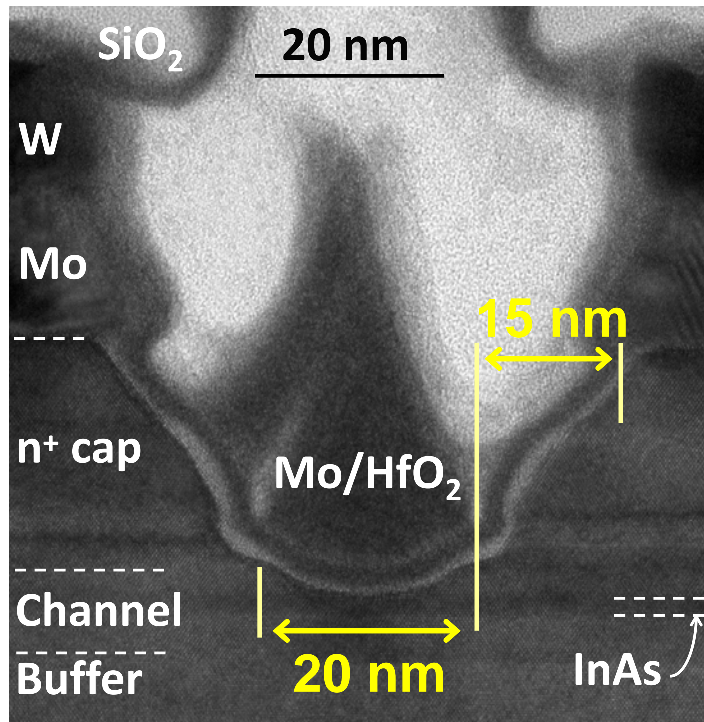
Finished device

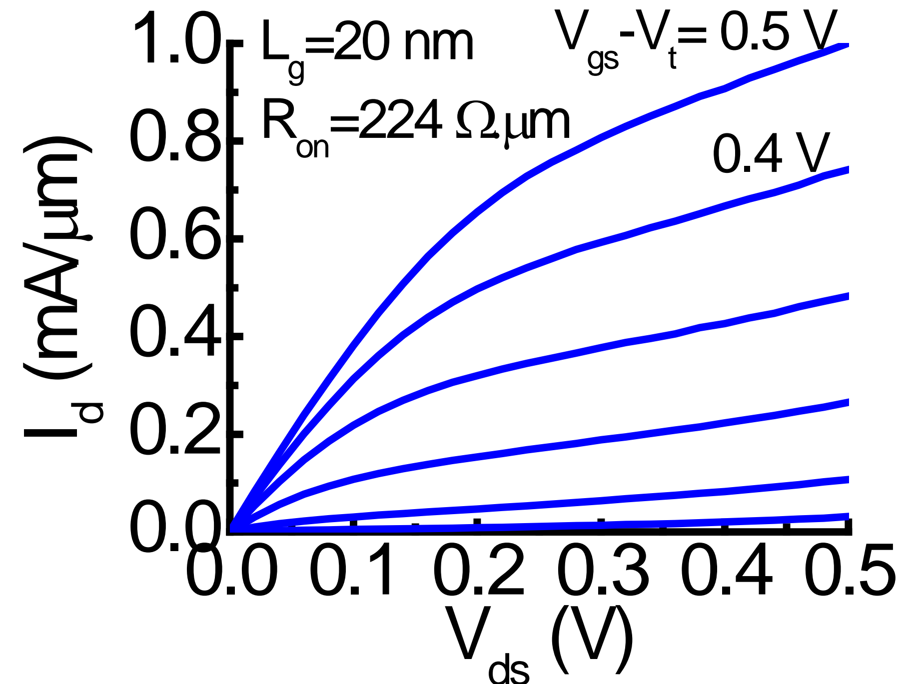


Lin, EDL 2014

- Ohmic contact first, gate last
- Precise control of vertical (~1 nm), lateral (~5 nm) dimensions
- MOS interface exposed late in process

L_g=20 nm InGaAs MOSFET





L_g = 20 nm, L_{access}= 15 nm MOSFET

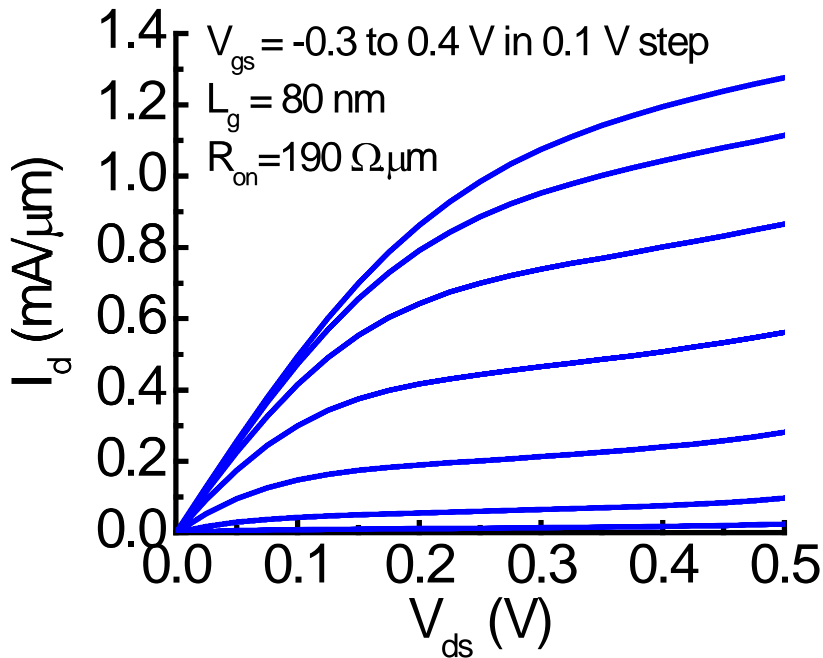
→ most compact III-V MOSFET made at the time

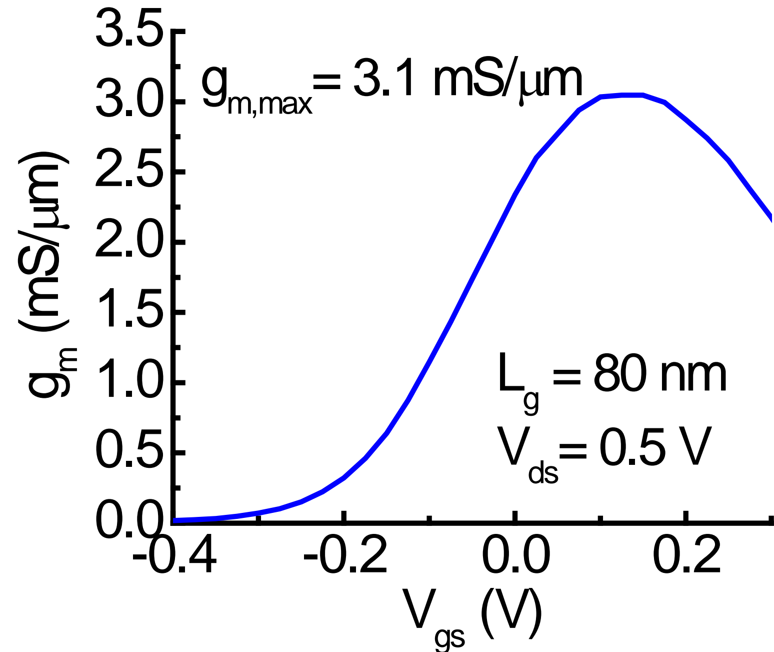
Lin, IEDM 2013

Highest performance InGaAs MOSFET

- Channel: $In_{0.7}Ga_{0.3}As/InAs/In_{0.7}Ga_{0.3}As$
- Gate oxide: HfO_2 (2.5 nm, EOT~ 0.5 nm)

L_g =80 nm, t_c=9 nm



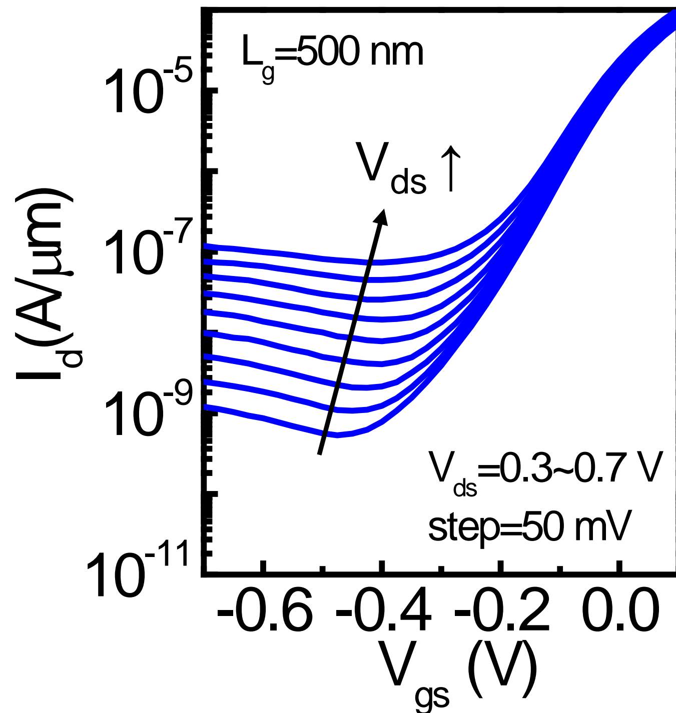


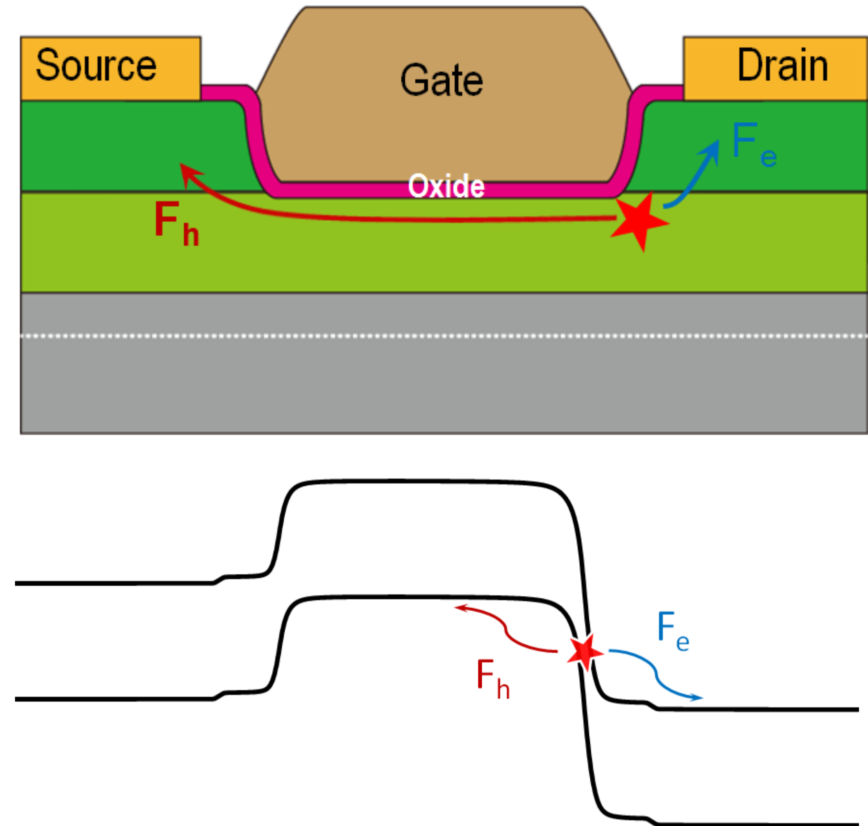
- Record $g_{m,max}$ = 3.1 mS/μm at V_{ds}= 0.5 V
- R_{on} = 190 Ω.μm

Lin, IEDM 2014

Excess OFF-state current

Transistor fails to turn off:



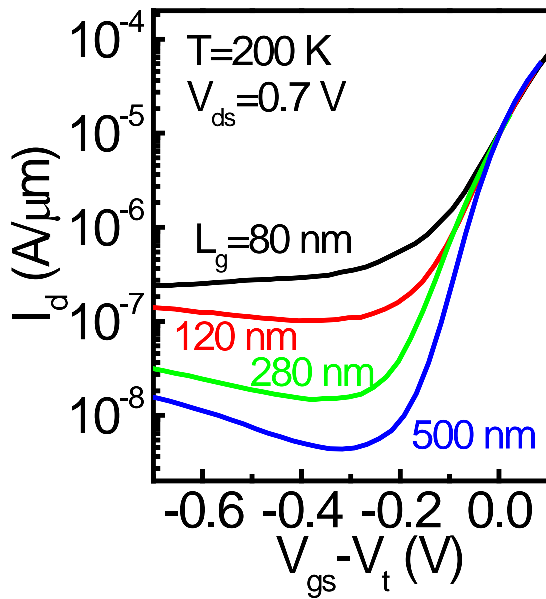


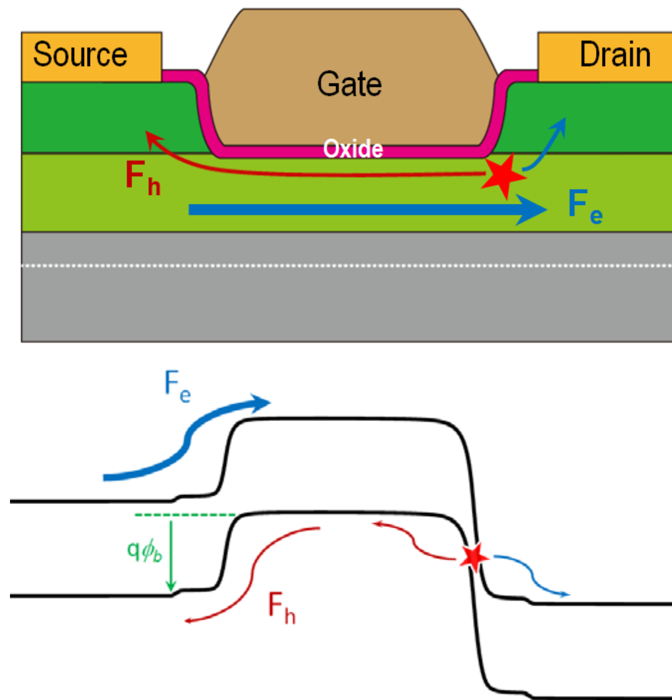
OFF-state current enhanced with V_{ds}

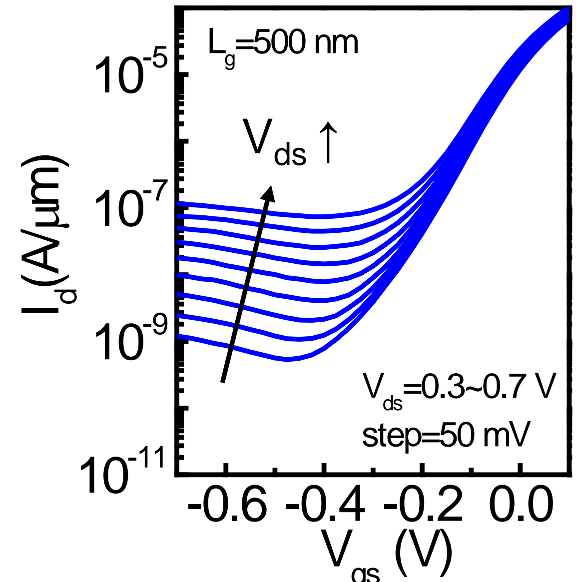
→ *Band-to-Band Tunneling (BTBT) or Gate-Induced Drain Leakage (GIDL)*

Lin, IEDM 2013

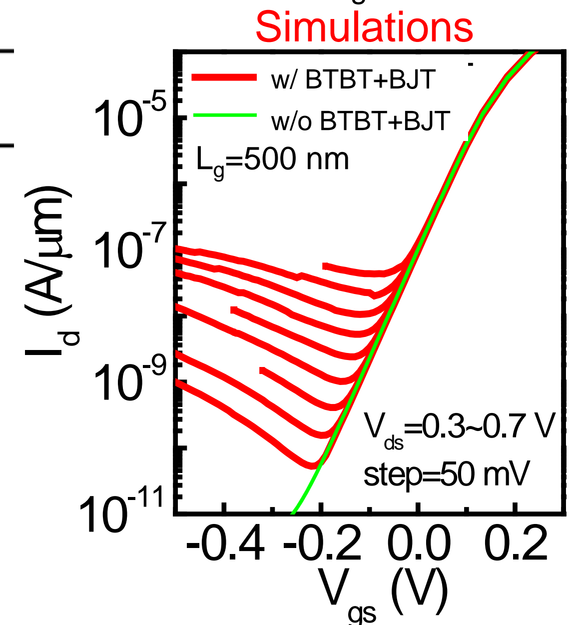
Excess OFF-state current







Simulations



Lin, EDL 2014

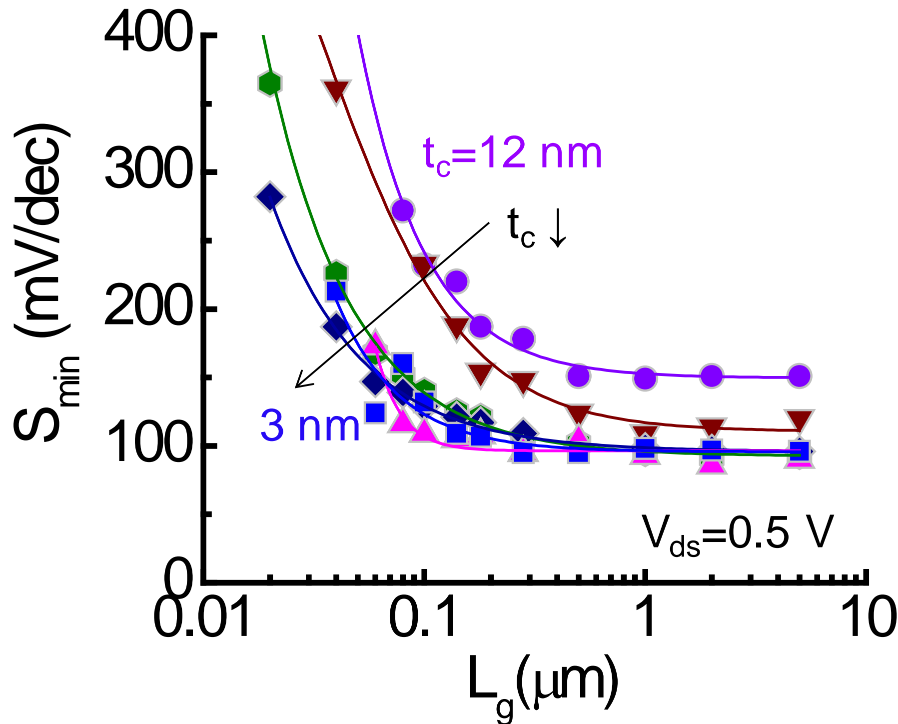
Lin, TED 2015

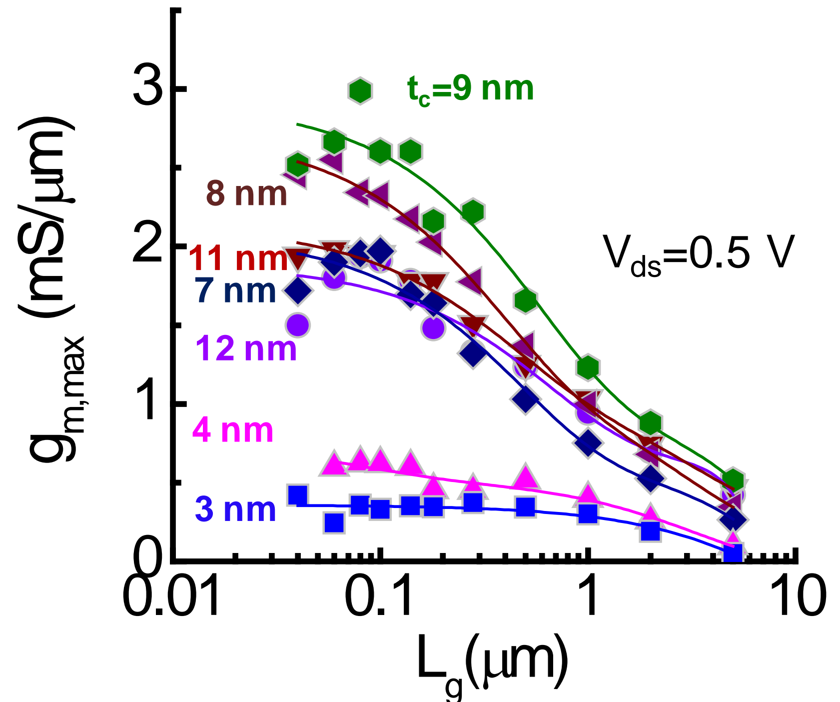
L_g↓ → OFF-state current ↑

→ additional *bipolar gain effect due to floating body*

Impact of channel thickness scaling

Lin, IEDM 2014
Lin, TED 2015



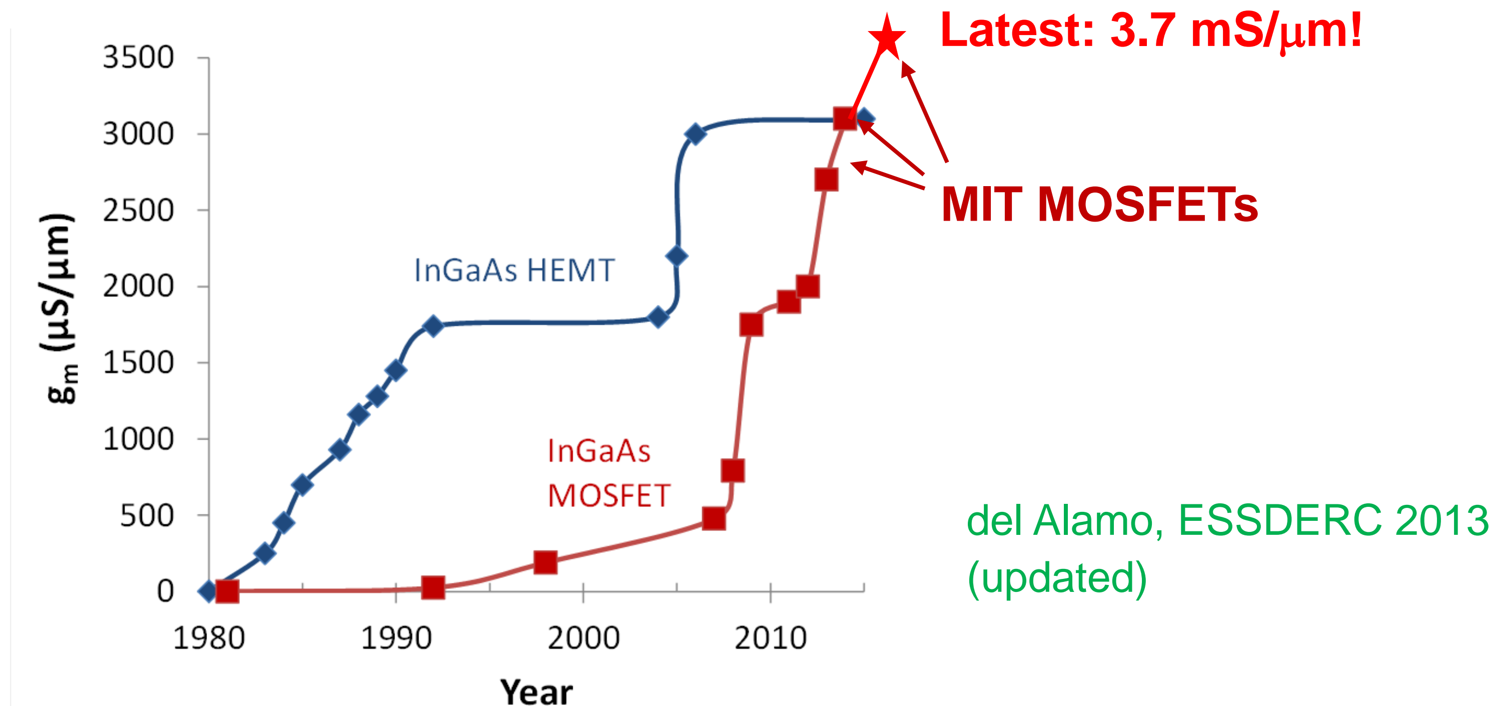


- t_c ↓ → S ↓ but also $g_{m,max}$ ↓
- Even at t_c=3 nm, $L_{g,min}$~40 nm

→ planar MOSFET at limit of scaling

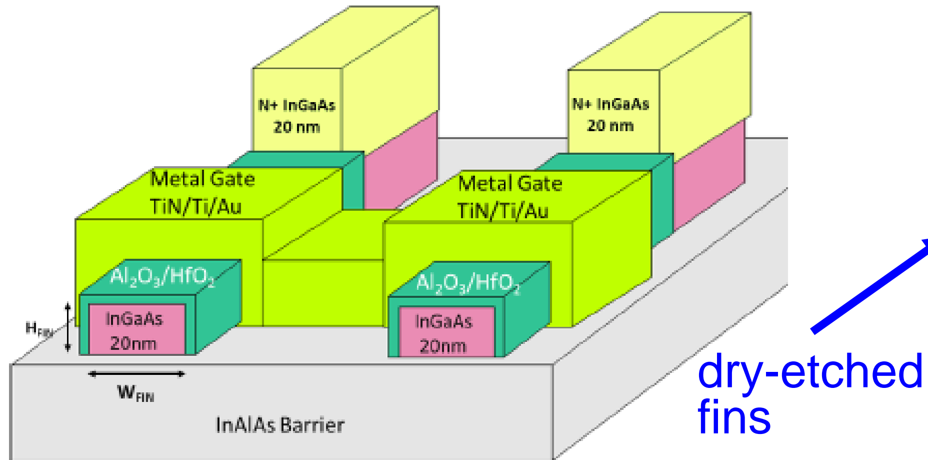
Benchmarking: g_m in MOSFETs vs. HEMTs

g_m of InGaAs MOSFETs vs. HEMTs (any V_{DD}, any L_g):

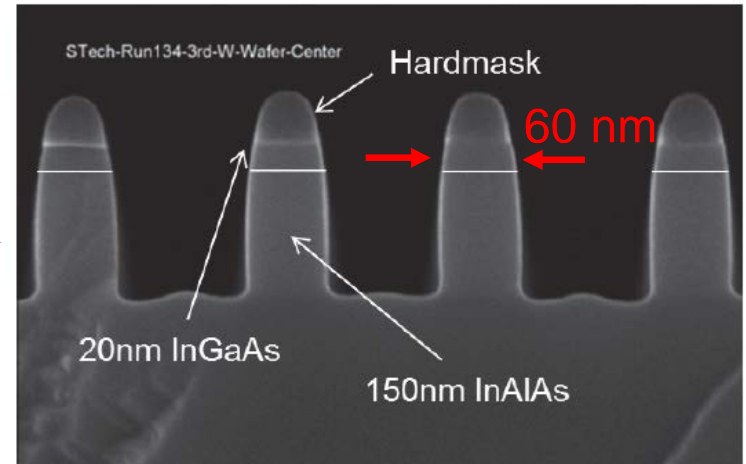


- Very rapid recent progress in MOSFET g_m
- Best MOSFETs now surpass best HEMTs
- No sign of stalling → more progress ahead!

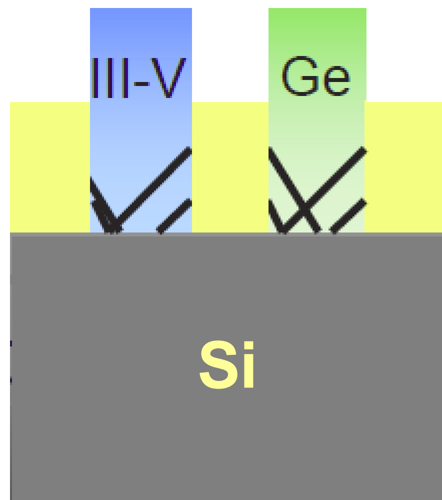
3. InGaAs FinFETs and Trigate MOSFETs



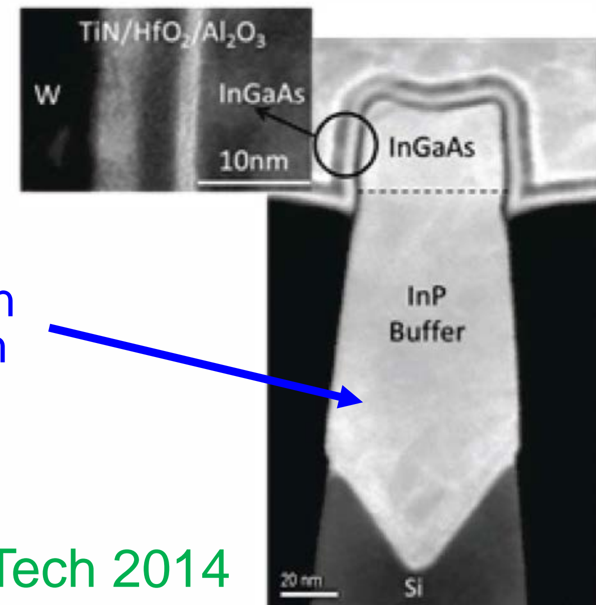
dry-etched fins



Kim, IEDM 2013



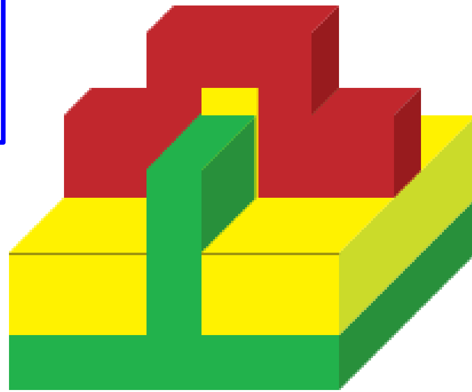
Epi-grown fin inside trench

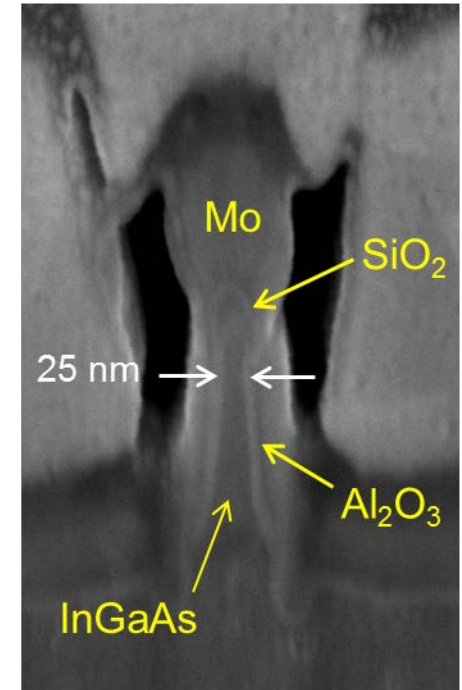


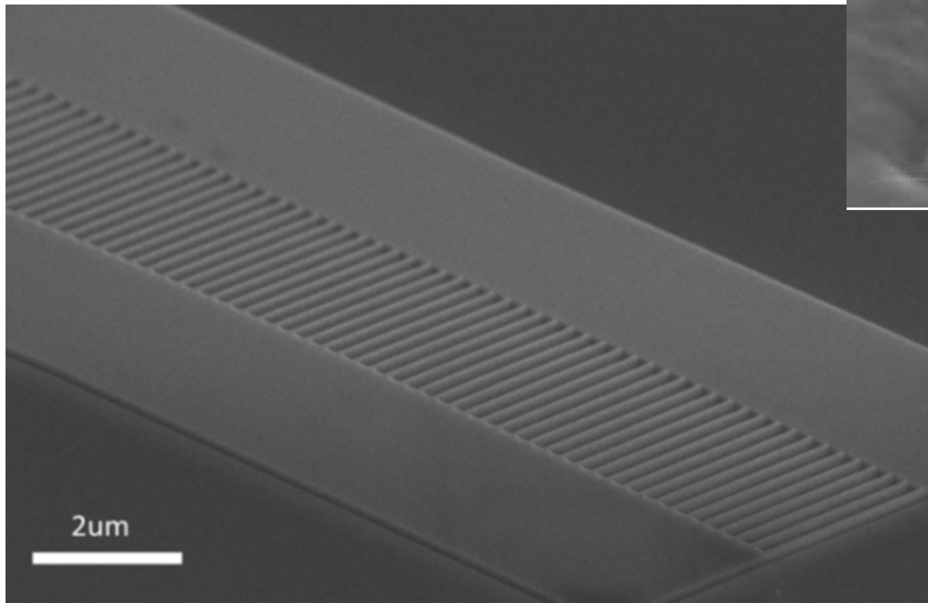
Waldron, VLSI Tech 2014

InGaAs FinFETs @ MIT

Alon Vardi







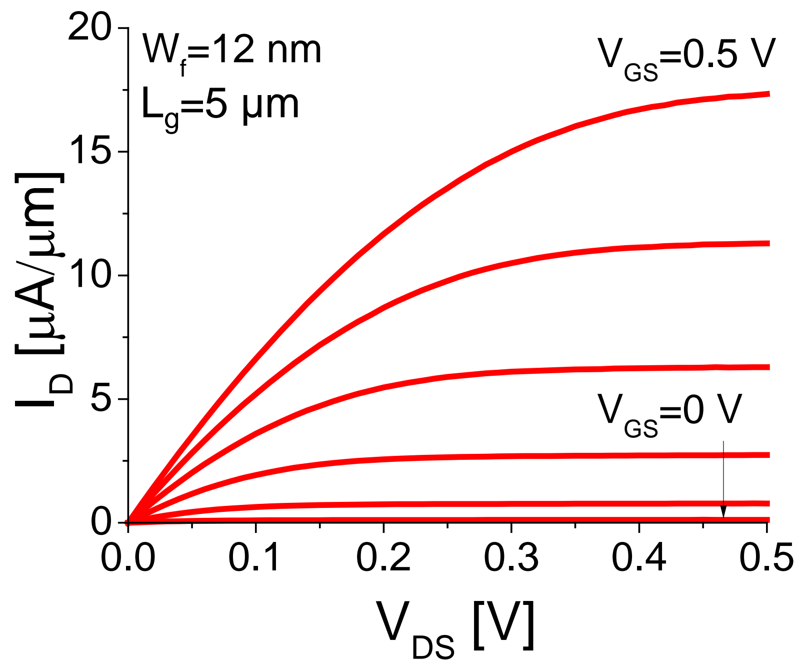
Key enabling technologies:

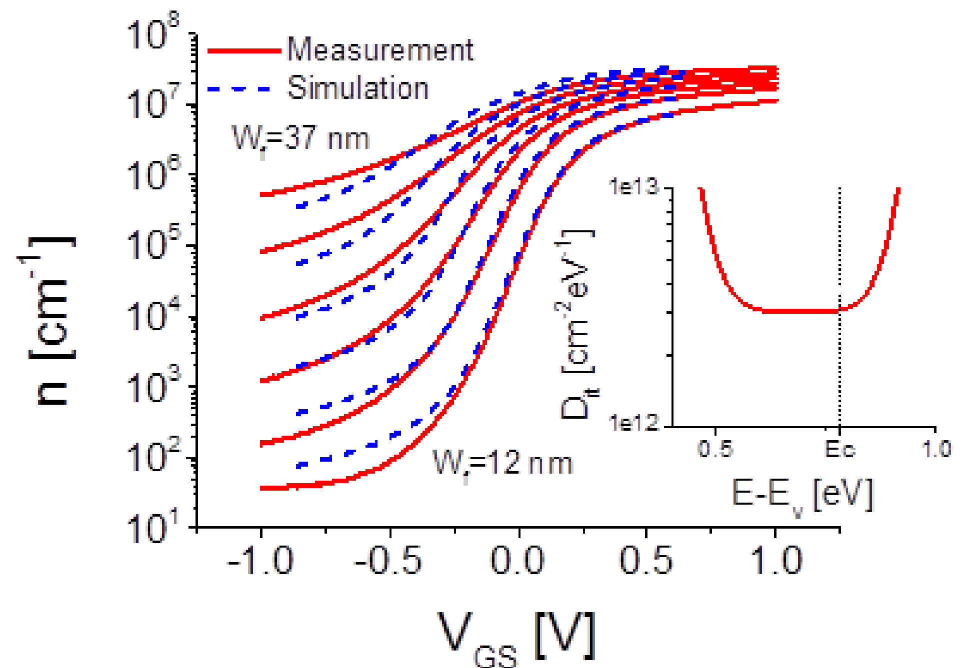
- $BCl_3/SiCl_4/Ar$ RIE
- digital etch

Zhao, EDL 2014; Vardi, DRC 2014

Interface-state study on sidewalls of InGaAs FinFET

Long-channel MOSFET characteristics (W_f=12~37 nm):





At sidewall: $D_{it,min}$ ~ $3x10^{12}$ $eV^{-1}.cm^{-2}$

Vardi, DRC 2014

Sub-10 nm fin width InGaAs FinFETs

InGaAs doped channel:

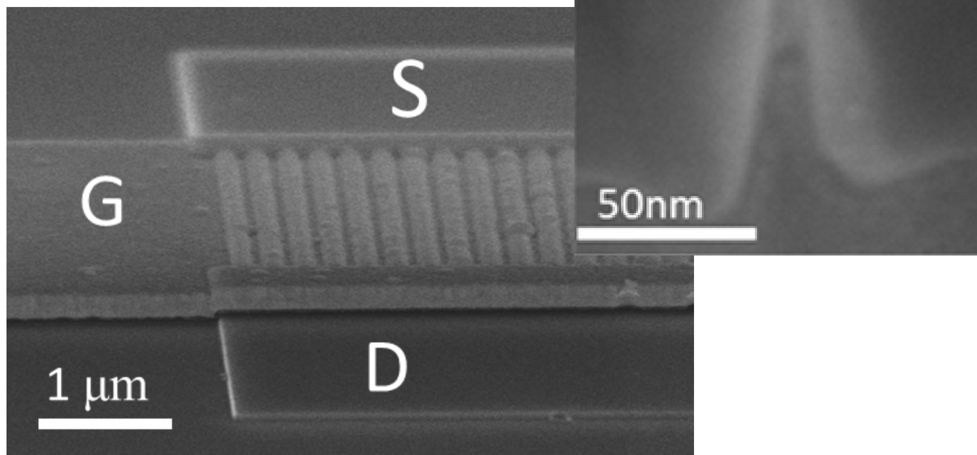
- 50 nm thick
- N_D~10^{18} cm^{-3}

Oxide: Al_2O_3/HfO_2 (EOT~3 nm)

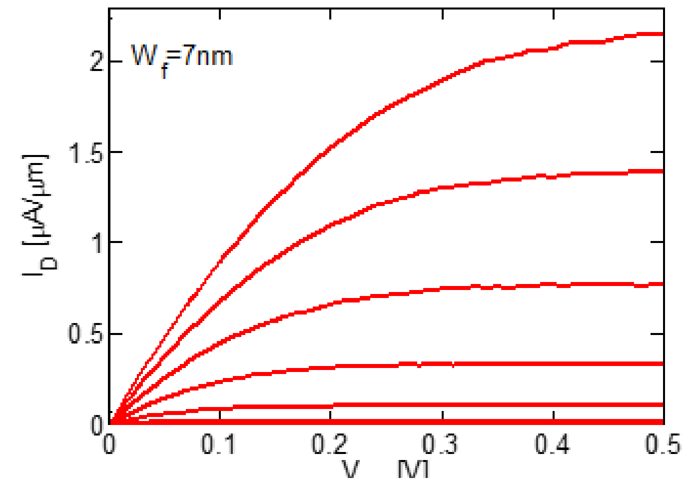
Fin width: 5 ~ 35 nm

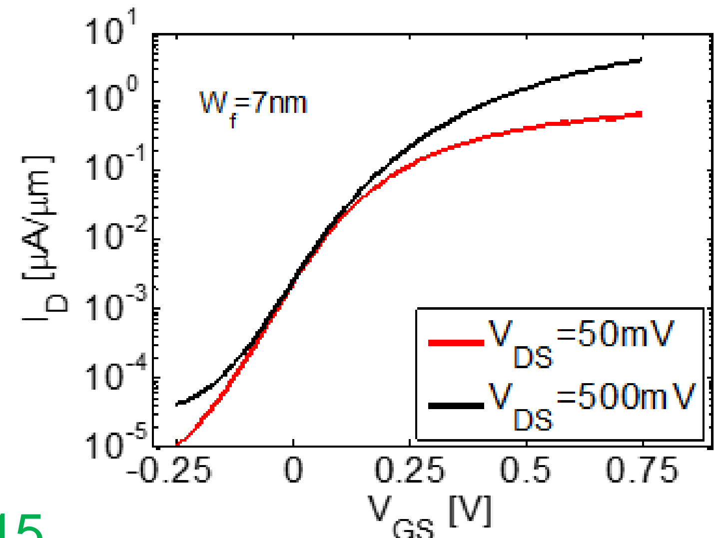
Fin height: 130 nm

100 fins



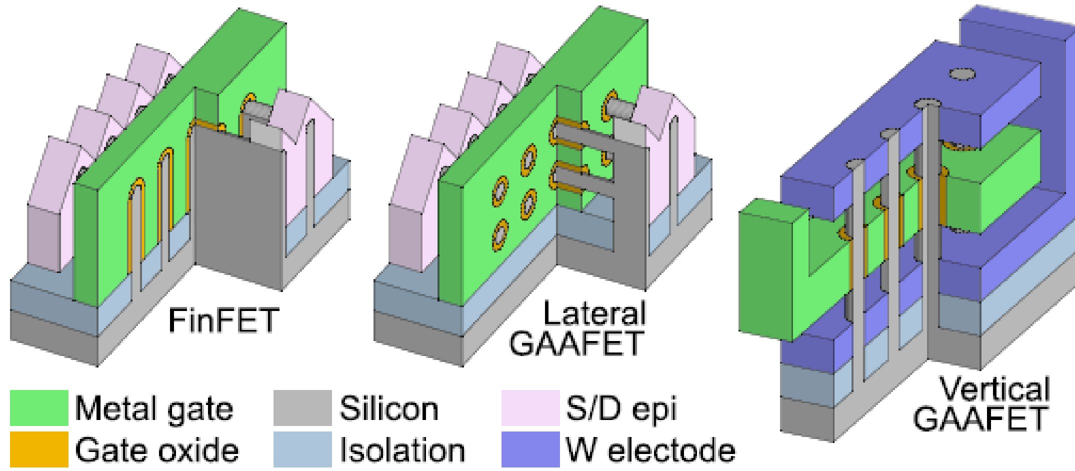
W_f=7 nm, L_g=3 μm MOSFET



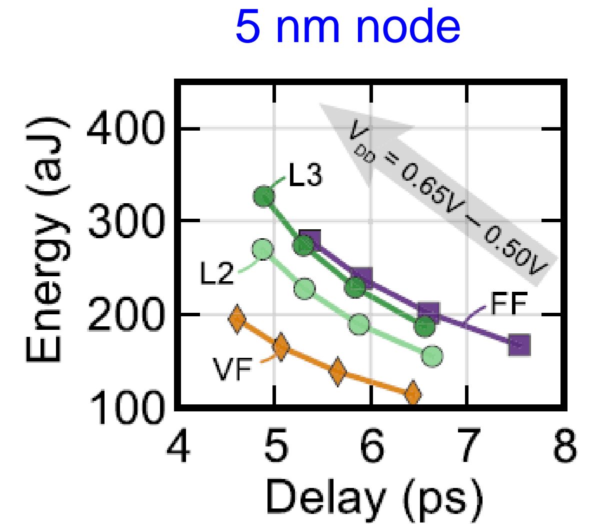


Vardi, IEDM 2015

4. Lateral vs. Vertical Nanowire MOSFETs

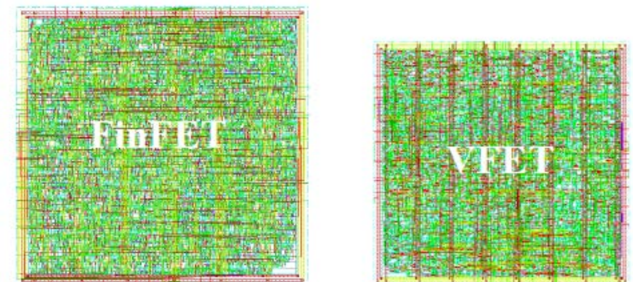


5 nm node



Yakimets, TED 2015
Bao, ESSDERC 2014

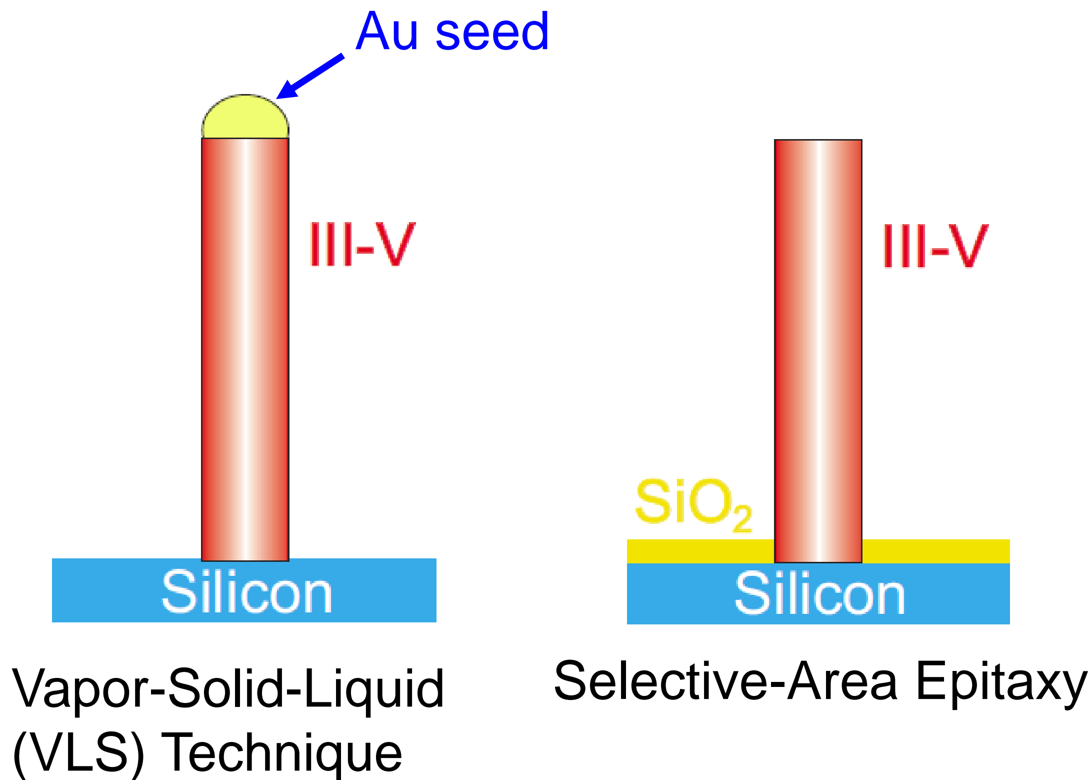
30% area reduction in 6T-SRAM
19% area reduction in 32 bit multiplier



- Nanowire MOSFET: ultimate scalable transistor
- Vertical NW: uncouples footprint scaling from L_g and L_c scaling

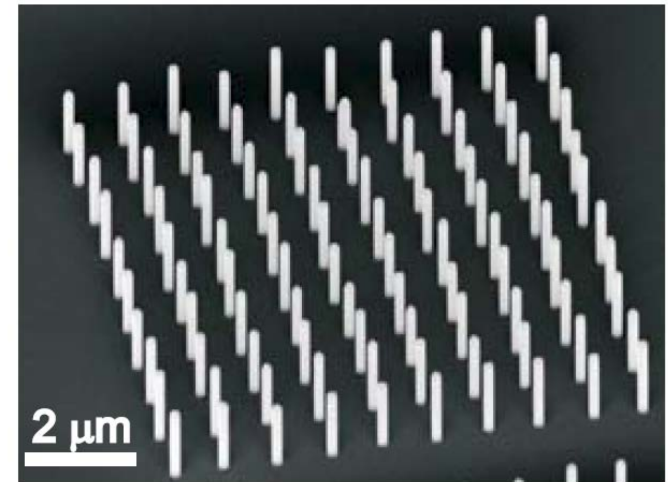
→ power, performance and area gains wrt. Lateral NW

InGaAs Vertical Nanowires on Si by direct growth

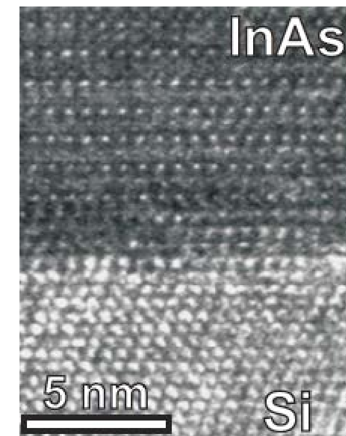


Vapor-Solid-Liquid (VLS) Technique

Selective-Area Epitaxy



InAs NWs on Si by SAE

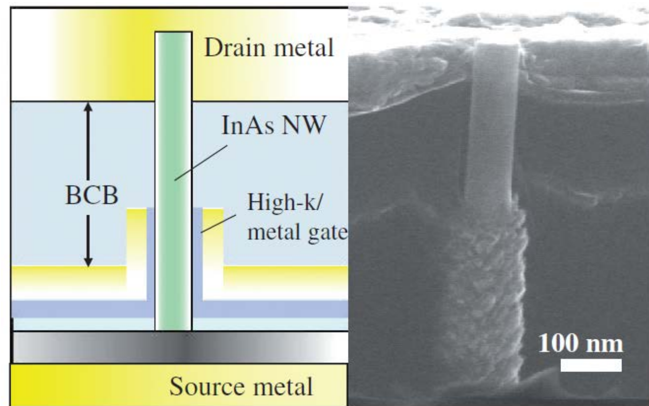


Riel, MRS Bull 2014

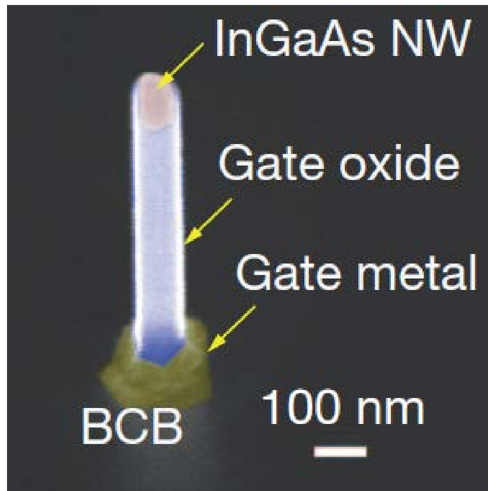
Björk, JCG 2012

InGaAs VNW-MOSFETs by *bottom-up* techniques

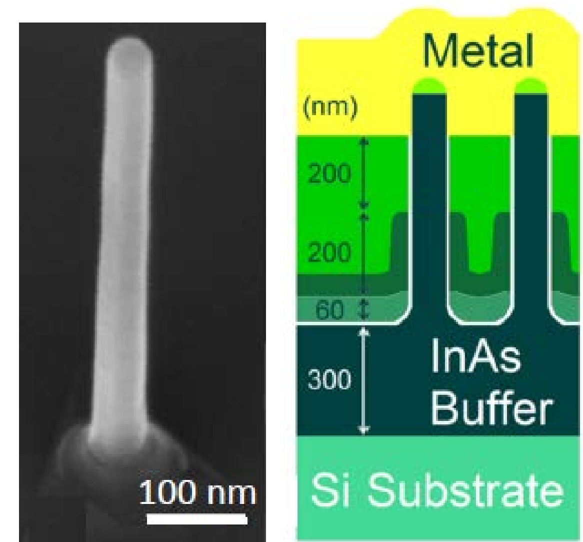
Many device demonstrations:



Tanaka, APEX 2010

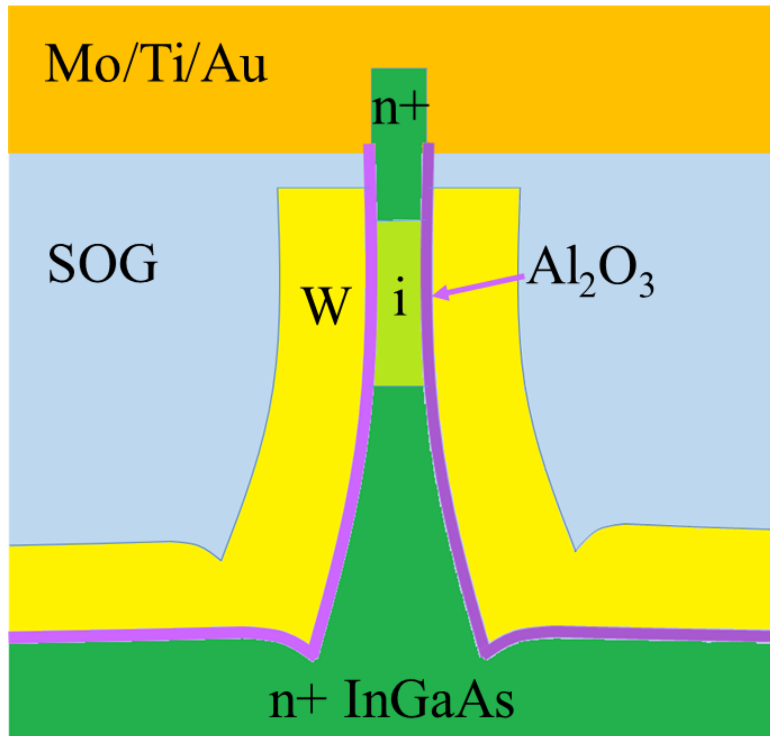


Tomioka, Nature 2012

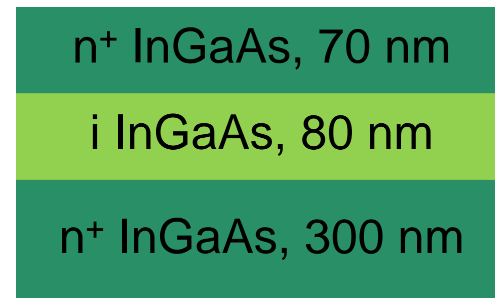


Persson, DRC 2012

InGaAs VNW-MOSFETs fabricated via top-down approach @ MIT



Starting heterostructure:

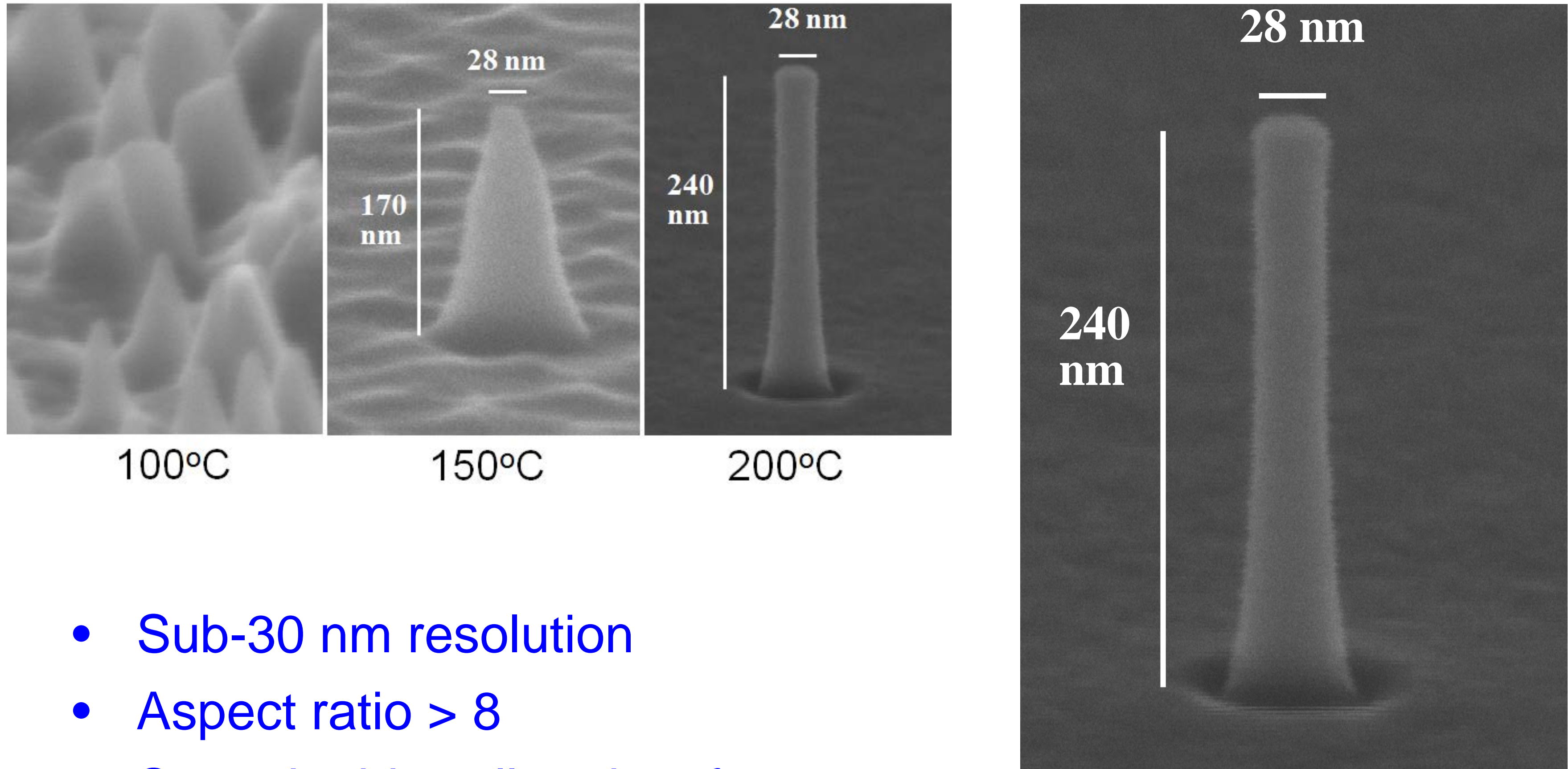


n^+: 6×10^{19} Si doping

Top-down approach: flexible and manufacturable

Zhao, IEDM 2013

Key enabling technology I:
RIE by $BCl_3/SiCl_4/Ar$ chemistry

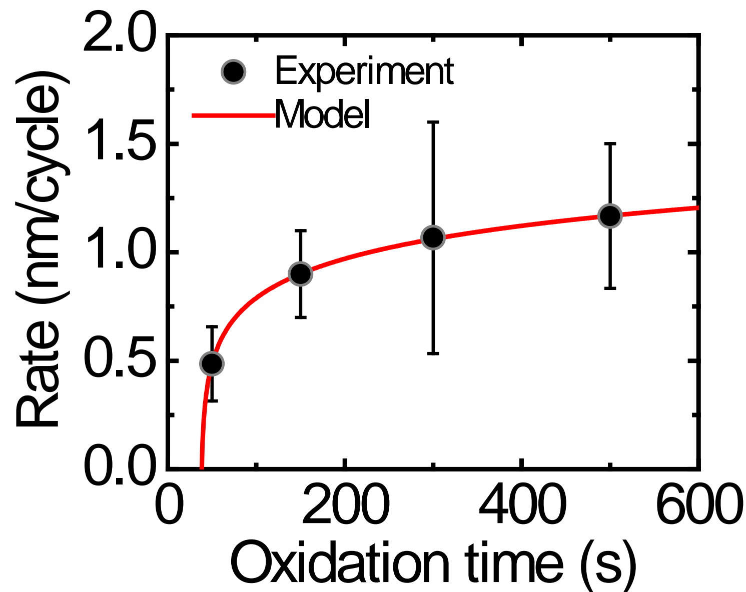


- Sub-30 nm resolution
- Aspect ratio > 8
- Smooth sidewall and surface
- Substrate temperature critical during RIE

Zhao, EDL 2014

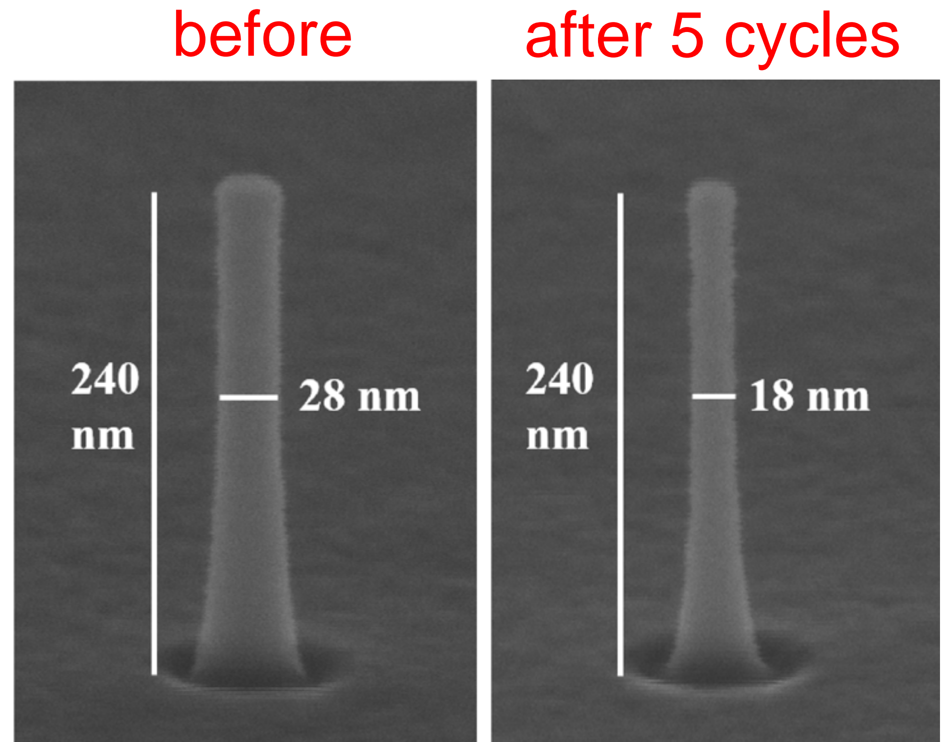
Key enabling technology II: digital etch

Self-limiting O_2 plasma oxidation + H_2SO_4 oxide removal



before

after 5 cycles

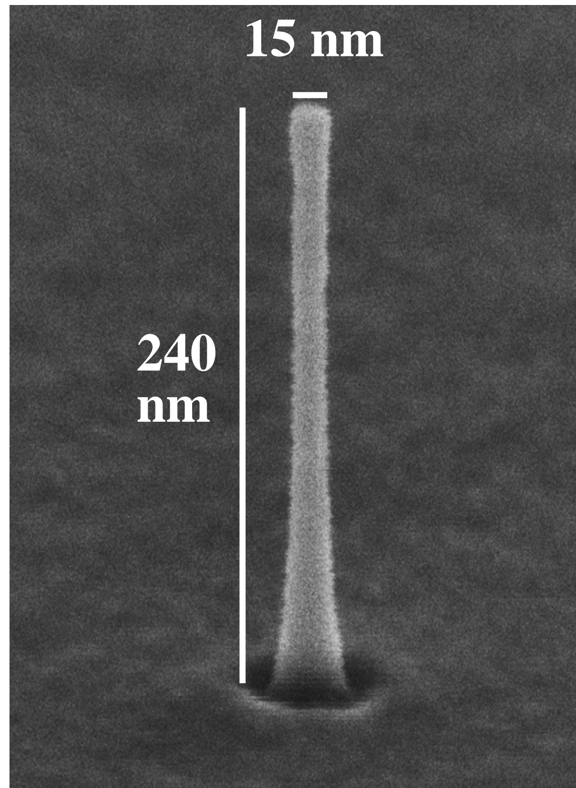


- Planar etching rate: ~1 nm/cycle
- Shrinks NW diameter by 2 nm per cycle
- Unchanged shape
- Reduced roughness

Lin, EDL 2014

Zhao, EDL 2014

Optimized RIE + Digital Etch

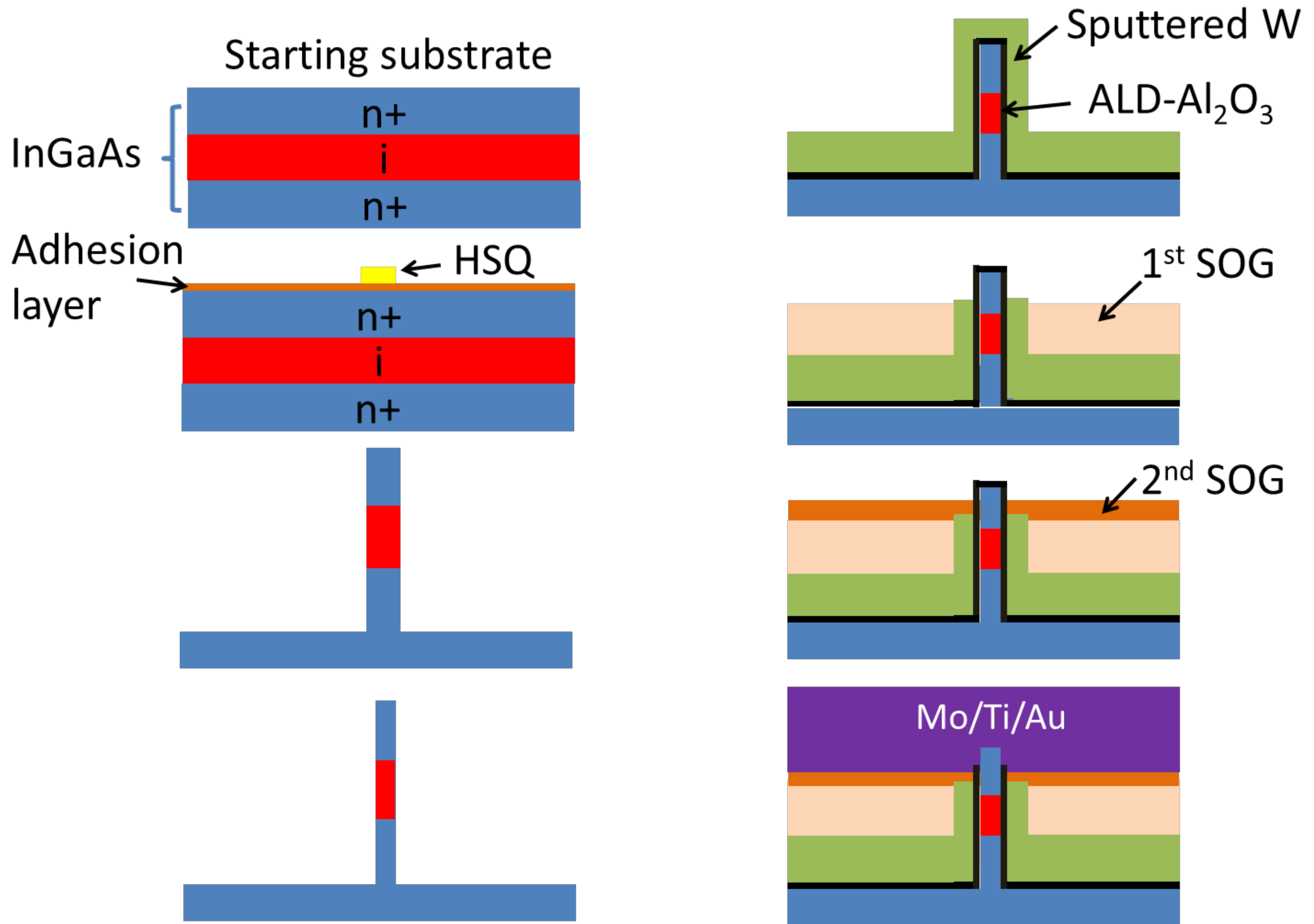


Zhao, EDL 2014

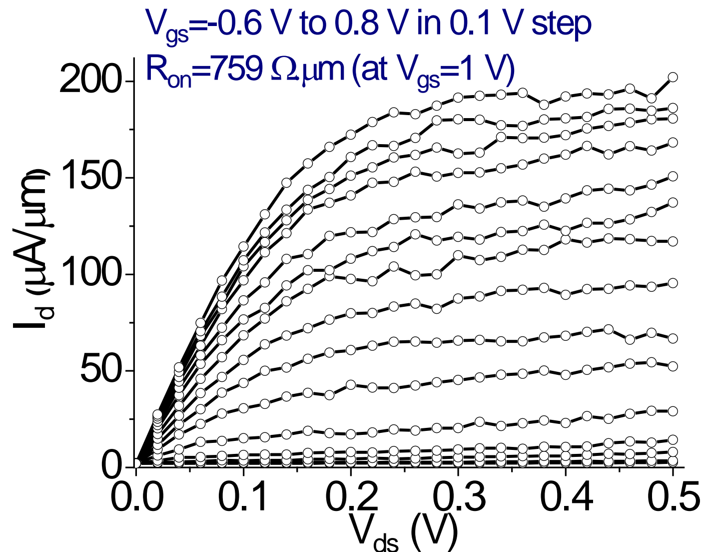
- Sub-20 nm resolution
- Aspect ratio = 16, vertical sidewall
- Smooth sidewall and surface

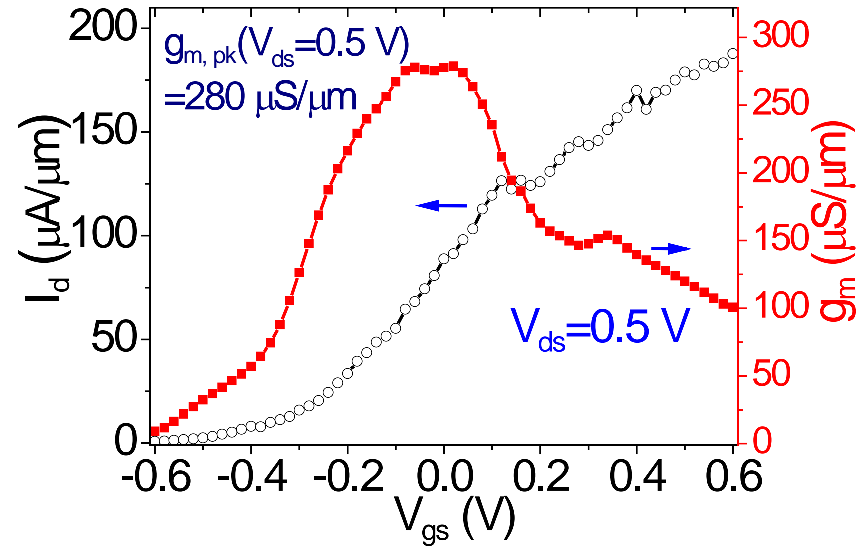
Tomioka, Nature 2012
Persson, DRC 2012

Process flow



NW-MOSFET I-V characteristics D=30 nm



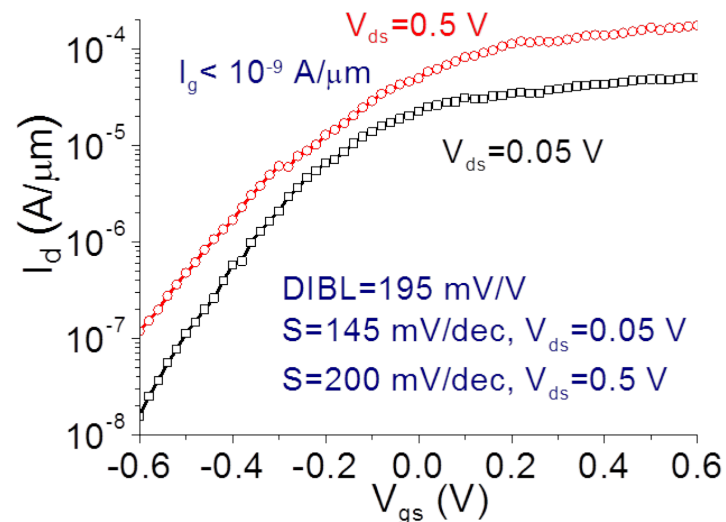


Single nanowire MOSFET:

- L_{ch}= 80 nm
- 4.5 nm Al_2O_3 (EOT = 2.2 nm)

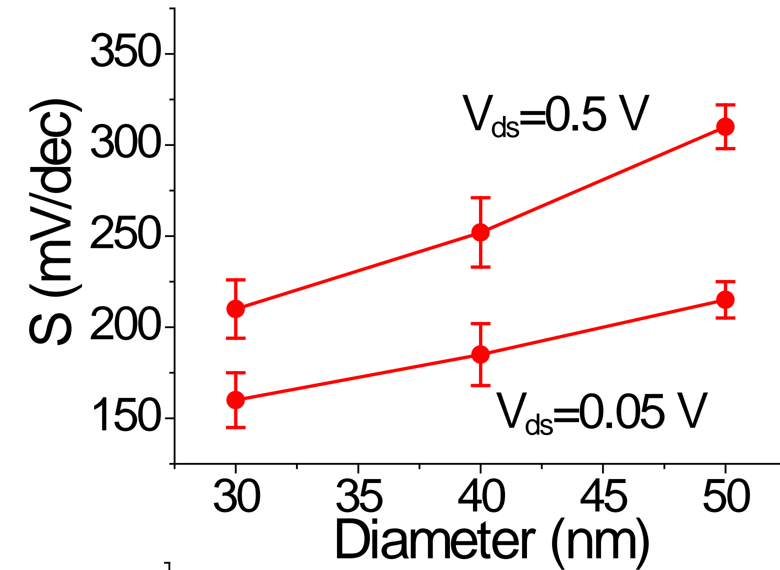
At V_{DS}=0.5 V:

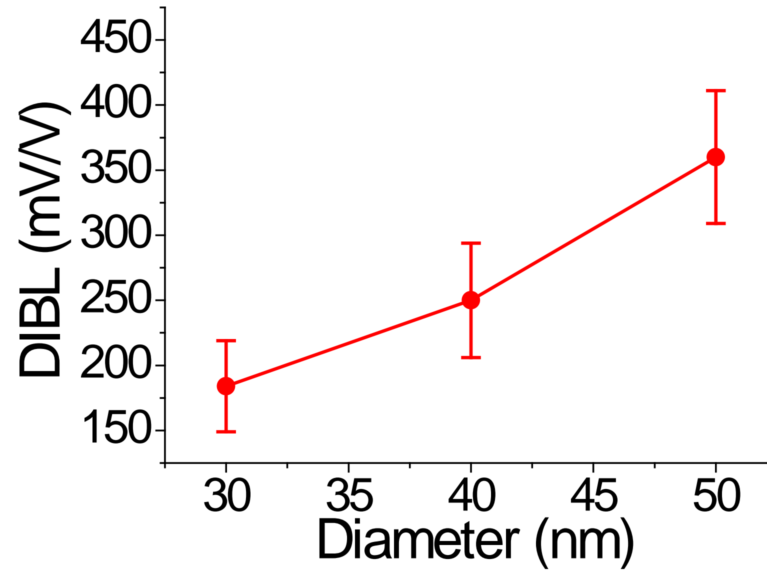
- $g_{m,pk}$=280 μS/μm
- R_{on}=759 Ω.μm

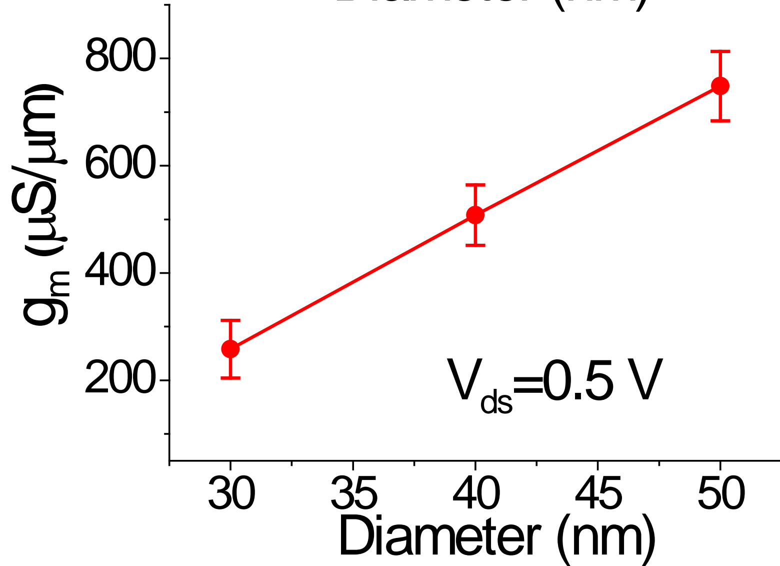


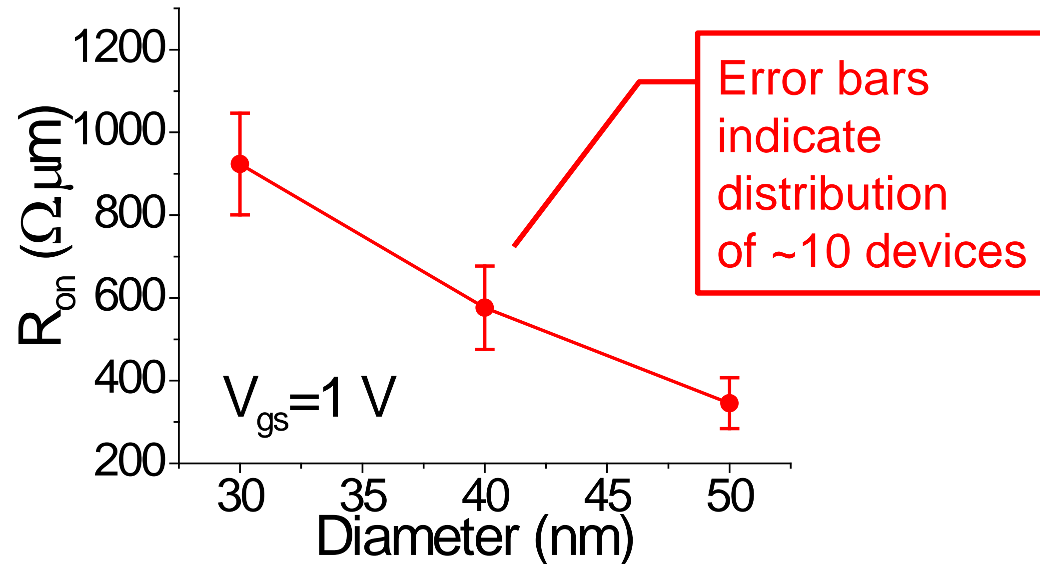
Zhao, IEDM 2013

Impact of nanowire diameter





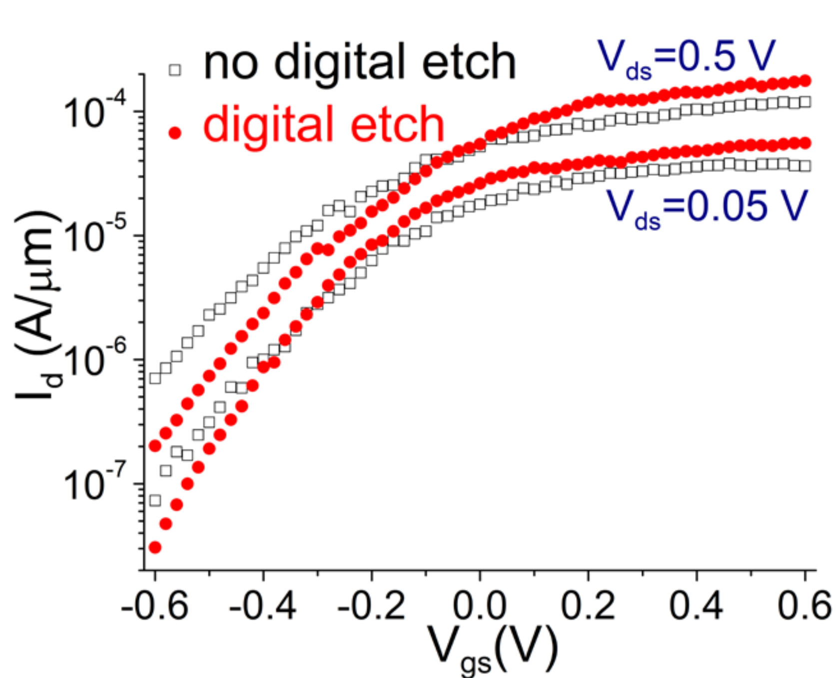


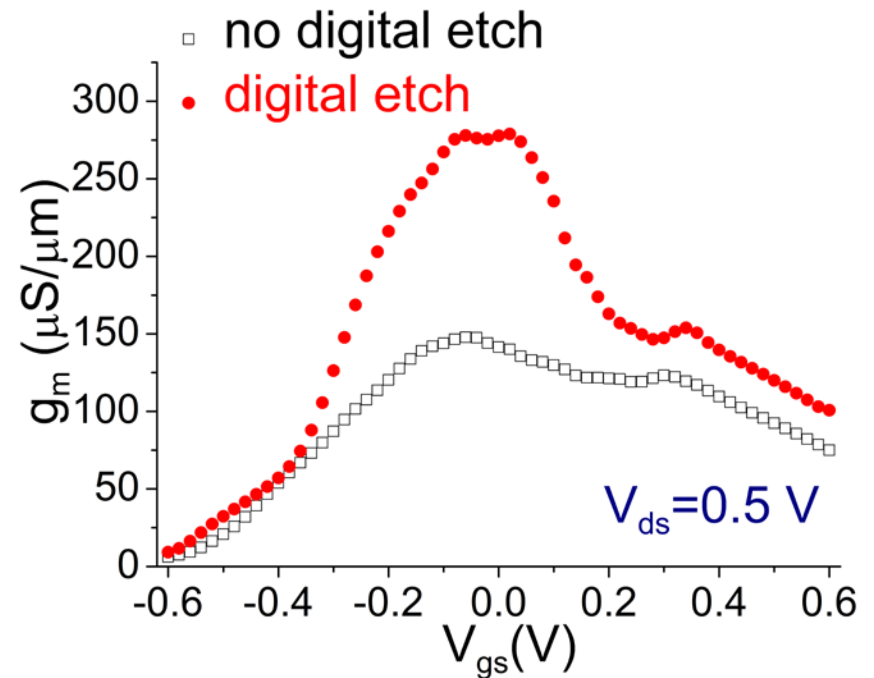


D↓ → S ↓, DIBL ↓, g_m ↓, R_{on} ↑

Impact of digital etch

Single nanowire MOSFET: D= 30 nm (final diameter)

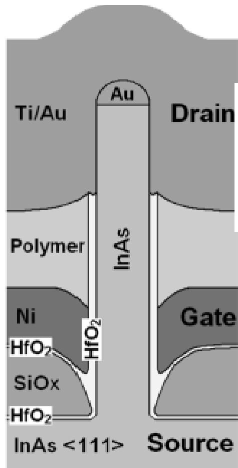




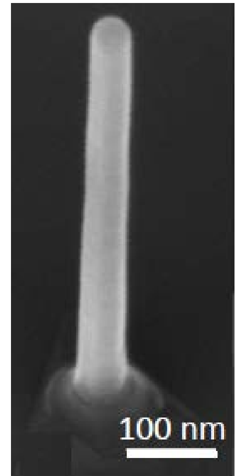
Zhao, EDL 2014

Digital etch → S ↓, g_m ↑ → Better sidewall interface

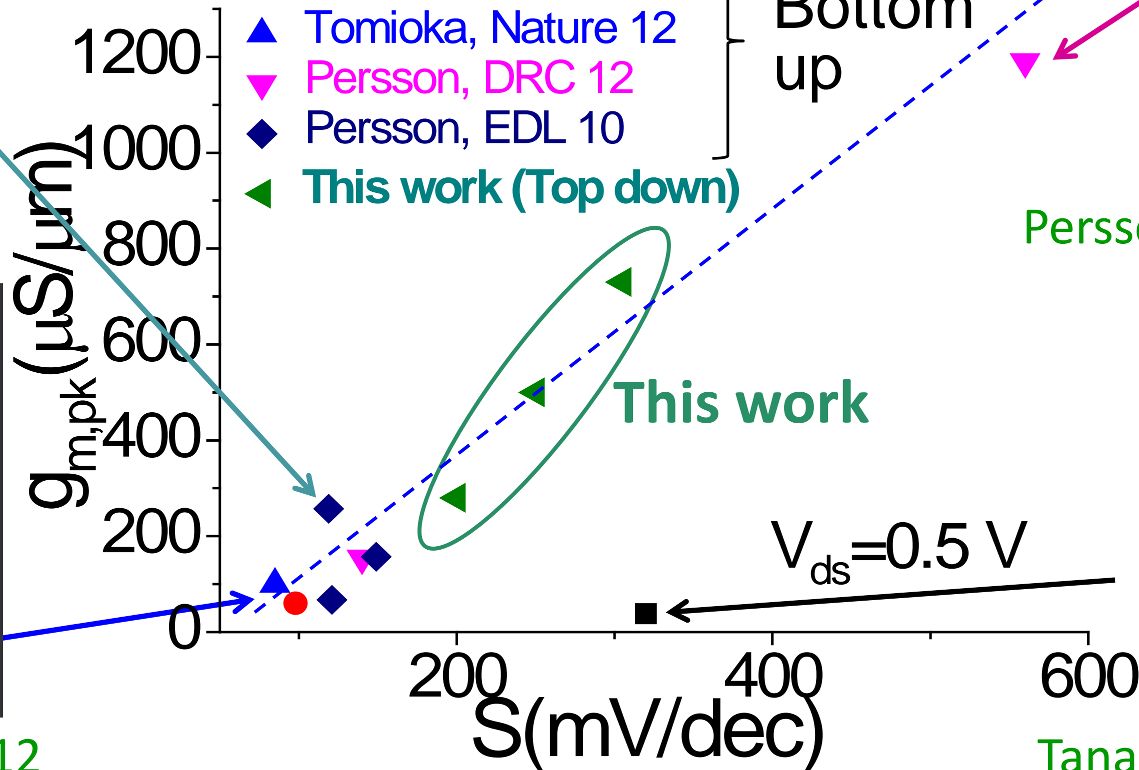
Benchmarking

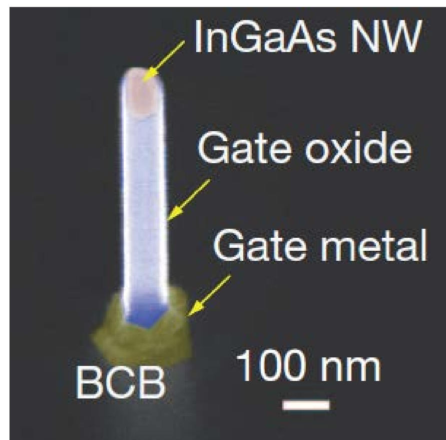


Persson, EDL 2012

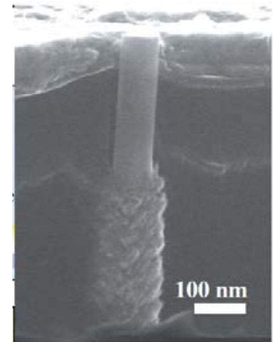


Persson, DRC 2012





Tomioka, Nature 2012

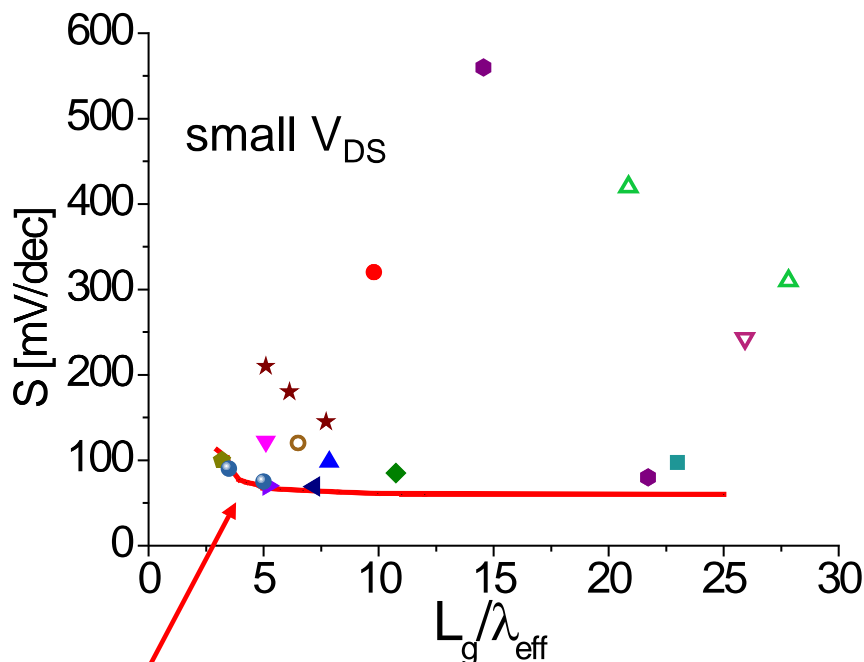


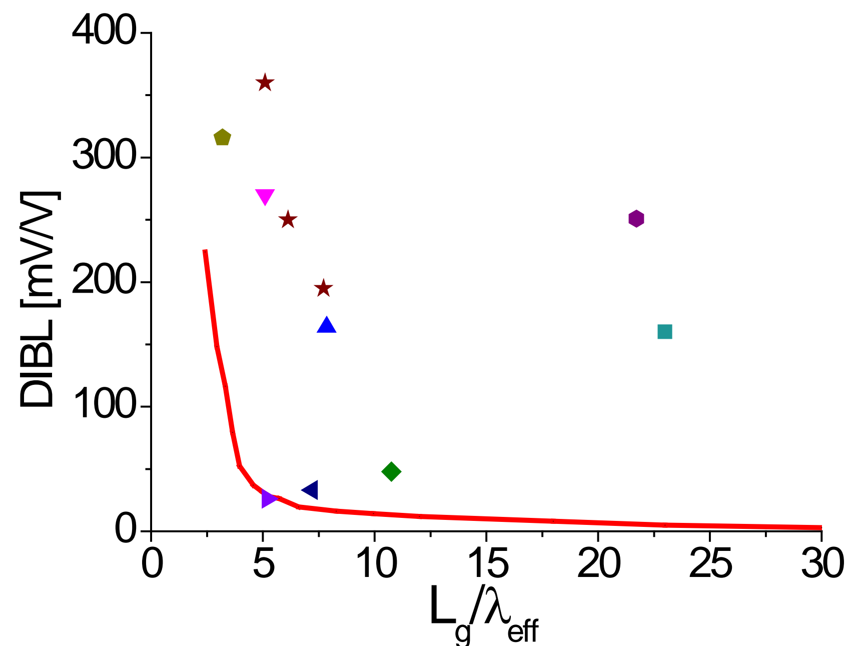
Tanaka, APEX 2010

- Trade-off: D↓ → S↓ but also g_m↓
- Top-down approach as good as bottom-up approach

InGaAs VNW MOSFET Concerns (a short list…)

- Relatively poor subthreshold behavior





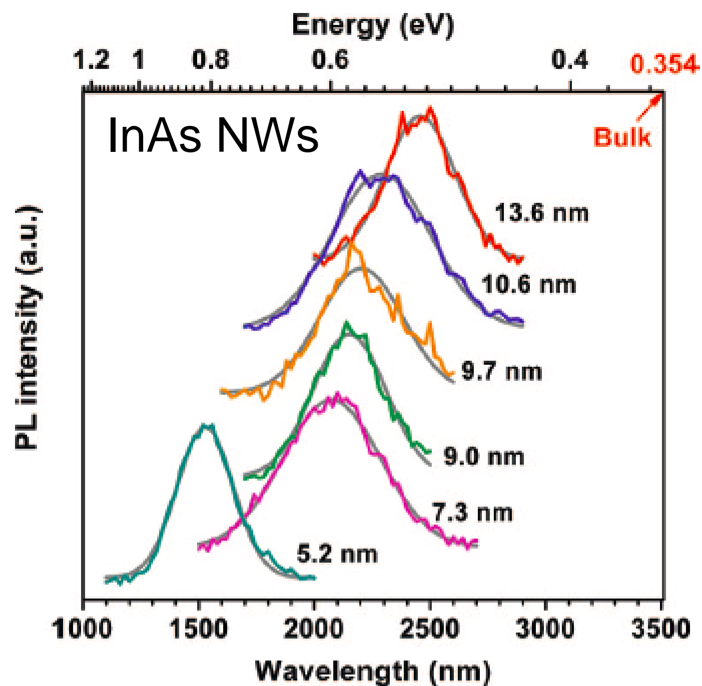
Auth, EDL 1997

$$\lambda_3 = \sqrt{\frac{2\varepsilon_{si} t_{si}^2 \ln\left(1 + \frac{2t_{ox}}{t_{si}}\right) + \varepsilon_{ox} t_{si}^2}{16\varepsilon_{ox}}}.$$

Electrostatic characteristic length for GAA NW

InGaAs VNW MOSFET Concerns (a short list…)

- Excess I_{off} due to BTBT + Floating BJT
  - → Quantization enhances bandgap
  - → Vertical bandgap engineering



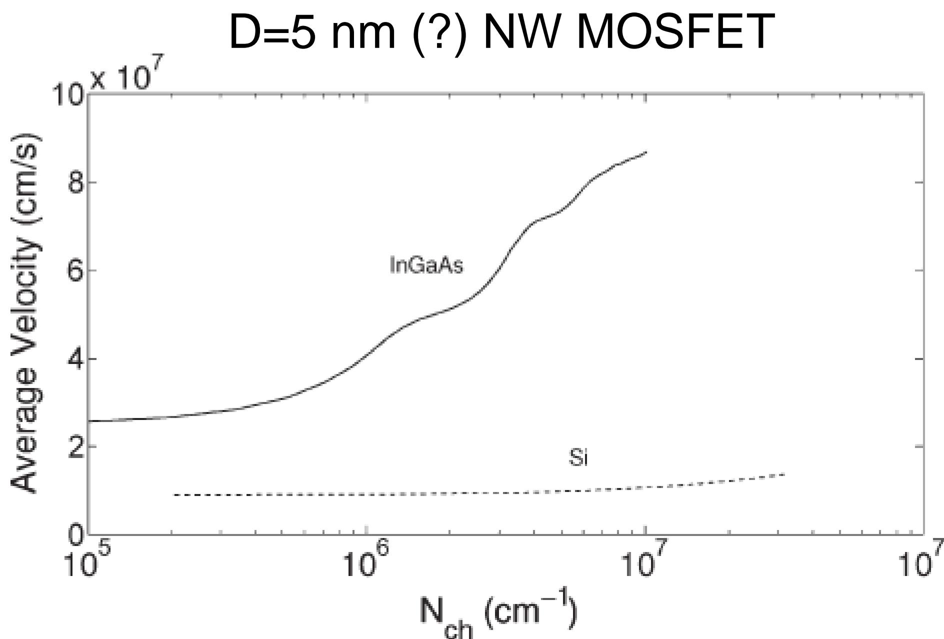
Wang, ACSNano 2008

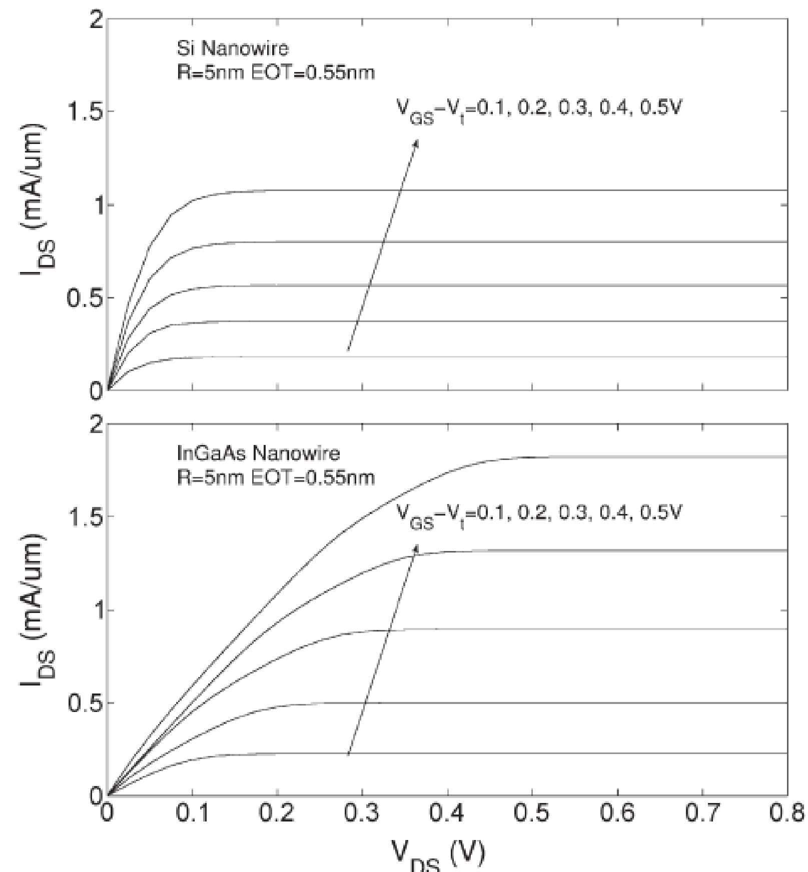
InGaAs VNW MOSFET Concerns (a short list…)

- InGaAs low DOS limits current

  → Increase in injection velocity with carrier density more than compensates for this

D=5 nm (?) NW MOSFET



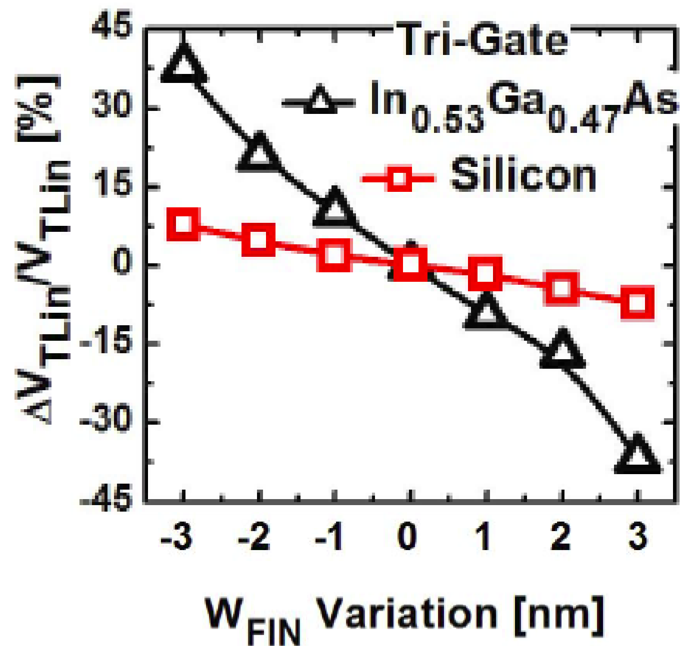


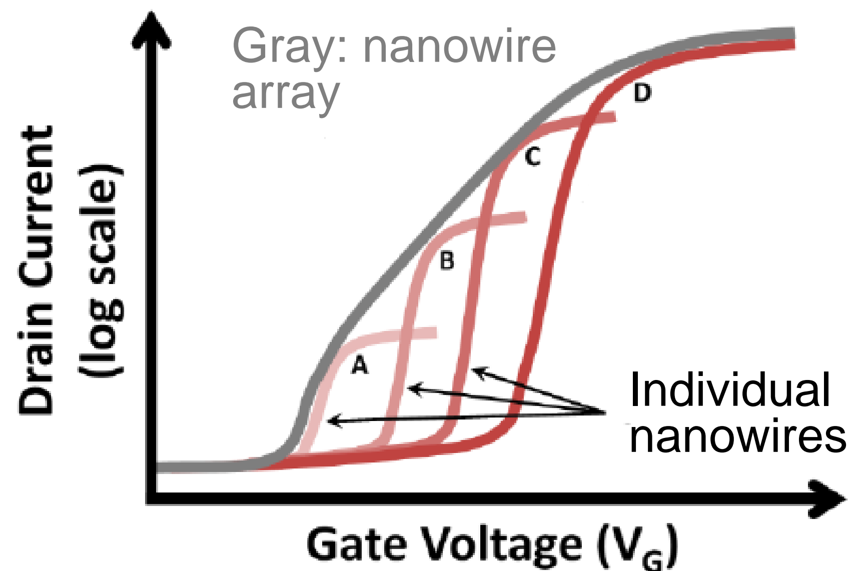
Yu, TED 2008

InGaAs VNW MOSFET Concerns (a short list…)

- V_T sensitivity to nanowire diameter
  → very tight manufacturing tolerance

W_f=8 nm Trigate MOSFETs



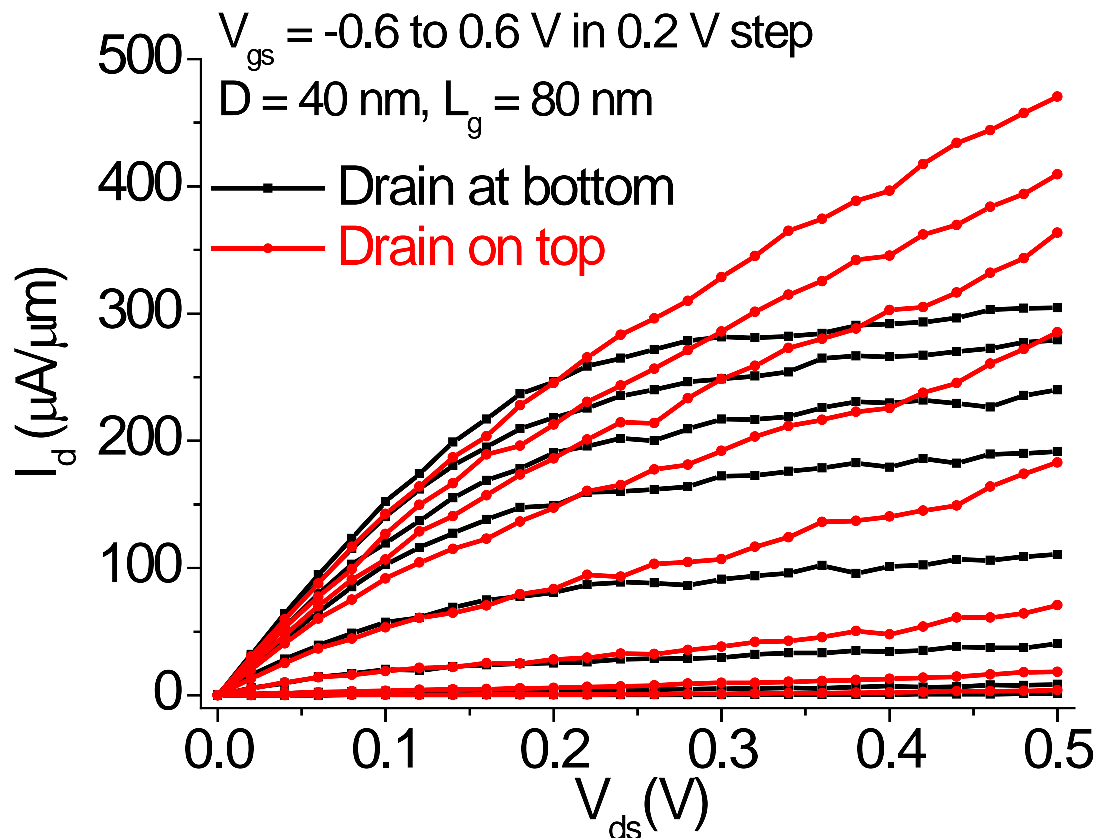


Agrawal, TED 2013

Teherani, PhD MIT, 2015

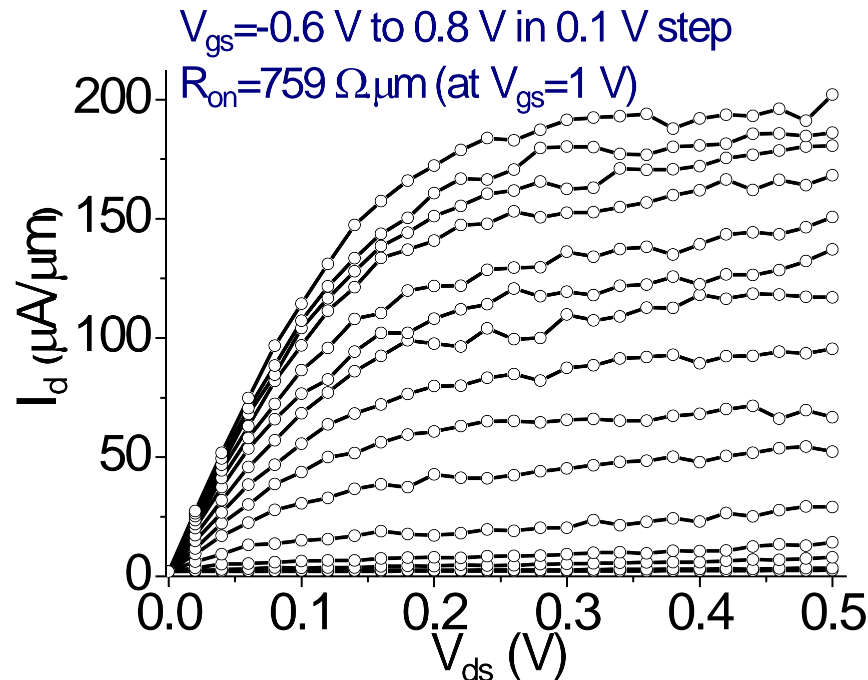
InGaAs VNW MOSFET Concerns (a short list…)

- Asymmetric device behavior: D down ≠ D up
  → more restrictive circuit wiring



InGaAs VNW MOSFET Concerns
(a short list…)

- Sensitivity to few defects



D=7 nm, L_g=14 nm (5 nm design rules)→ S_g=540 nm^2

D_{it}=2x10^{11} $cm^{-2}.eV^{-1}$ → N_{it}~1 eV^{-1}

InGaAs VNW MOSFET Concerns (a short list…)

- Top contact resistance
- Difficult to introduce mechanical stress
- Self-heating
- …

Conclusions

1. Great recent progress on planar, fin and nanowire III-V MOSFETs
2. Vertical Nanowire III-V MOSFET: superior scalability and power/performance characteristics
3. Vertical Nanowire n- and p-type III-V MOSFET: plausible path for co-integration on Si
4. Many demonstrations of InGaAs VNW MOSFETs by bottom-up and top-down approaches
5. Many issues to work out:
   - sub-10 nm diameter nanowire fabrication, self-aligned contacts, device asymmetry, Introduction of mechanical stress, V_T control, device variability, BTBT and parasitic HBT gain, trapping, self-heating, reliability, co-integration with p-type VNW on Si, …

A lot of work ahead but…
exciting future for III-V electronics